APPLICATION OF SELENIUM RECTIFIERS AS SWITCHING DEVICES IN THE MARK II CALCULATOR

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THE APPLICATION OF SELENIUM RECTIFIERS AS SWITCHING DEVICES IN THE MARK IV CALCULATOR

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PREFACE

Selenium rectifiers as switching or control devices were first systematically employed in the construction of Mark IV Calculator. This machine, designed and constructed by the Staff of the Computation Laboratory for the Flight Research Laboratory of the United States Air Force, is presently in an advanced test stage, and should enter upon production computation in the very near future. The use of selenium rectifiers as switching devices in connection with calculator design was proposed by Professor Howard Aiken, and has given satisfactory results in applications dealing with Storage Systems, Arithmetic Units, and Sequence Control Units. The investigations leading to these applications were carried out by several members of the Staff including the present writer. In particular, the design of the Slow Storage and Sequence Units of Mark IV were prepared by him and are treated in detail in Chapters 3 and 4 of this thesis. These chapters will be preceded by a more general discussion of rectifier circuits.

The author wishes to express his appreciation to Professor Aiken for the opportunity to carry out these investigations and for his encouragement and advice, which have greatly contributed to the completion of this work. Further, he is grateful to various members of the Staff of the Computation Laboratory for their assistance and criticism. Finally, he is indebted to Miss Helene Thoman for her assistance in innumerable tasks which were required in the design and testing of the Slow Storage and Sequence Units and in the preparation of this manuscript, and to Mrs. Floyd Wilkins, Jr. for preparing this text for printing.

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SYNOPSIS

Selenium rectifiers with an active area of about 0.0005 square inch have been available commercially since World War II. The rectifiers can safely pass a forward current of 0.4 MA and can be used with a back voltage of 18 V. The capacitance of the rectifiers is estimated at 70 μμF. The small size of the rectifiers and their low cost make them admirably suited for use in switching circuits of a large size.

Rectifiers can be combined in circuits which perform the logical "and" operation or the logical "or" operation. It is possible to use the output of an "and" circuit as an input to an "or" circuit and vice versa. This kind of switching circuit is generally known. An analysis of the circuit which is obtained when small selenium rectifiers are used shows that the application of this kind of rectifier to switching circuits is limited by the speed of the rectifier circuits. An average decay time of 2 microseconds and a rise time of 6 microseconds restrict the use of selenium rectifier circuits to medium speed operations. The use of selenium rectifiers as the main switching element in circuits which operate with a pulse time of 20 microseconds or more was first suggested by Professor Howard H. Aiken.

It is possible to combine as many as 10 input signals in one "and" circuit and to have as many as 25 "and" conditions combined in one "or" circuit. The circuit which combines "and" conditions by means of one "or" condition is only one of a variety of rectifier circuits. The conditions which occur most frequently in large systems are of the type "and-or," as is shown by the example of the rectifier circuits of the Mark IV Calculator. Ninety-six percent of the rectifier circuits used

in this system are of the type "and-or." The size of the rectifiers makes it possible to build the entire "and-or" circuit in one small unit.

The output of a rectifier circuit differs in amplitude, waveform and impedance from the input supplied to the circuit. In order to be able to use the signal output again as an input to other circuits an amplifier and cathode follower are added to the rectifier circuit. The circuit thus obtained can be considered the basic unit of a switching circuit. This unit is very powerful in representing the logical conditions which occur in large switching circuits. Such a circuit can be considered as a large network of signal wires. Each signal originates from a basic unit and is used in turn to control other units. A system of this kind will contain several closed loops. An investigation of small systems with a feedback loop shows that it is possible to combine two basic units in a circuit with two stable states. This circuit shows a great resemblance to a conventional trigger pair. However, it makes use of less vacuum-tubes and can be controlled much more conveniently. In general, n units can be combined in a circuit with nCm stable states, where m is the number of outputs which is low in each state. The expression nCm represents the number of combinations m at a time of n quantities. These circuits are called multiplets and can be used to store information. They are particularly convenient because the conditions which are to be stored can be used to control the multiplets without any intermediate circuits. It is furthermore possible to make a read-in to a multiplet dependent upon the state of the multiplet when the read-in occurs. A multiplet of the type nC(n-1) can in this way step through its n states in any desired order. This principle can be extended to a group of multiplets which control each other, so that their outputs will assume in succession a desired number of states. Such a group of multiplets has been called a ring. While there are many known

examples of rings using triode or pentode trigger pairs, it is believed that the multiplets and the rings of multiplets form an original contribution. A valuable characteristic of the basic switching unit and the circuits which can be derived from it is that more than one operation can be performed by the circuit. Because of this it is possible for a ring to step through more than one cycle, each cycle being controlled by a separate condition.

The application of multiple state circuits which use selenium rectifiers is limited by the speed with which the circuit can change its state. It has been verified experimentally that for small multiplets a time of 2 microseconds is required to perform the change over. An application of the circuits which have been developed is given in the description of the Sequence Unit and the Slow Storage Unit of Mark IV. The major parts of these units consist of rectifier switching circuits. It can be noted that it is possible to perform a large variety of more or less complicated operations conveniently with rectifier circuits. Furthermore it is possible to represent the conditions which are involved in each of these operations in a uniform and systematic way. In total 328 basic switching units are used in these circuits. The number of trigger pairs which is used is 163. The design of the Slow Storage Unit shows the application of multiplets of the type 302 and 502. The use of rings of multiplets is illustrated by four examples each consisting of four trigger pairs. The experience which has been obtained during the 8 months that the circuits have been observed in actual operating condition shows that the rectifiers are highly reliable. The possibility of using selenium rectifier circuits is an important argument in favor of switching systems which use a medium speed.

CHAPTER 1

SELENIUM RECTIFIER SWITCHING CIRCUITS

A. Characteristics of Selenium Rectifiers

Rectifier Action

The contact surface between crystalline selenium and a metal alloy has a conductivity which is a function of the magnitude and direction of the current passed through the surface. The conductivity for a current passing from the selenium to the metal is large compared with the conductivity which is observed for a current in the opposite direction. The operation of selenium rectifiers is based on this phenomenon. A cross-section of a selenium rectifier is shown in Fig. 1-1. A steel or aluminum

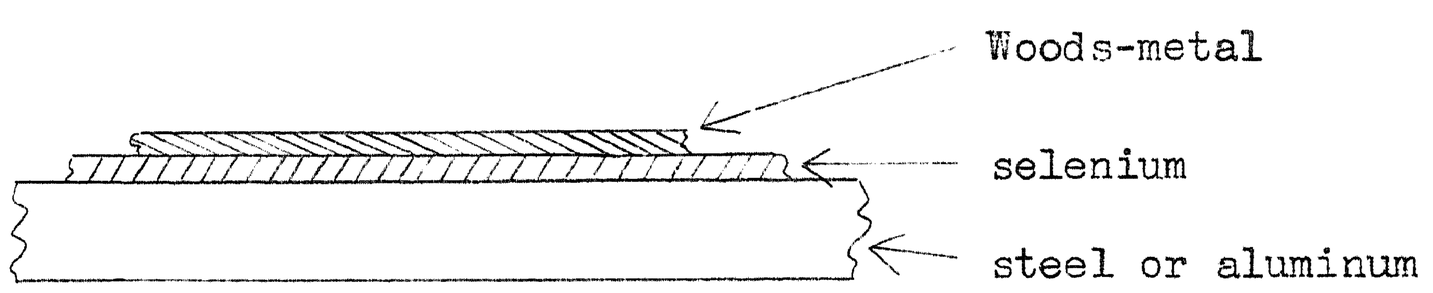

Fig. 1-1. Cross-Section of a Selenium Rectifier

plate serves as a base for the selenium layer. This plate is the anode of the cell. Besides giving mechanical strength to the unit, the plate serves to conduct the heat developed in the cell. The selenium layer is pressed or evaporated onto the base plate. It is heat-treated to obtain its crystalline form and subsequently sprayed with the counter electrode metal. An alloy with a low melting point, such as Woods-metal, is used for the counter electrode. Because of the spraying operation a surface

contact, rather than a point contact, is obtained between the selenium and the cathode. Thus the conductivity of a selenium rectifier is directly proportional to the active area of the cell.

Voltage-Current Curve

Figure 1-2 shows the voltage-current curve for a small size selenium rectifier. This curve is representative for operation of the rectifiers used in the circuits of the Mark IV Calculator. The active area of these rectifiers is of the order of 0.0005 square inch. With 2 V applied in the forward conducting direction, the current through the rectifier is 0.5 MA. The part of the curve which shows the back conducting properties of the rectifier has been drawn on a larger scale. The current begins to increase appreciably around -20 V. This limits the back voltage which can be applied. The back resistance of a selenium rectifier can be increased by means of a forming process. This process consists of the application of voltage pulses in the back direction. An unfiltered rectified alternating current can be used for this purpose. When this voltage is applied, the back current through the rectifier decreases slowly. The voltage is subsequently increased until finally a state of near constant current and voltage is obtained. The rectifier retains the larger back resistance which has been obtained in this manner. The voltage at which the back current begins to increase is -40 V for a formed rectifier. When a rectifier is used in a switching circuit it will be subject to pulses in the back direction which have a lower voltage than those used for forming. They result in a less effective forming process. The lasting changes in forward or back conducting characteristics are known as aging. Each voltage applied to the rectifier will also produce a temporary change, called creep. Thus the instantaneous characteristic of a selenium rectifier is at all times a function of its past history.

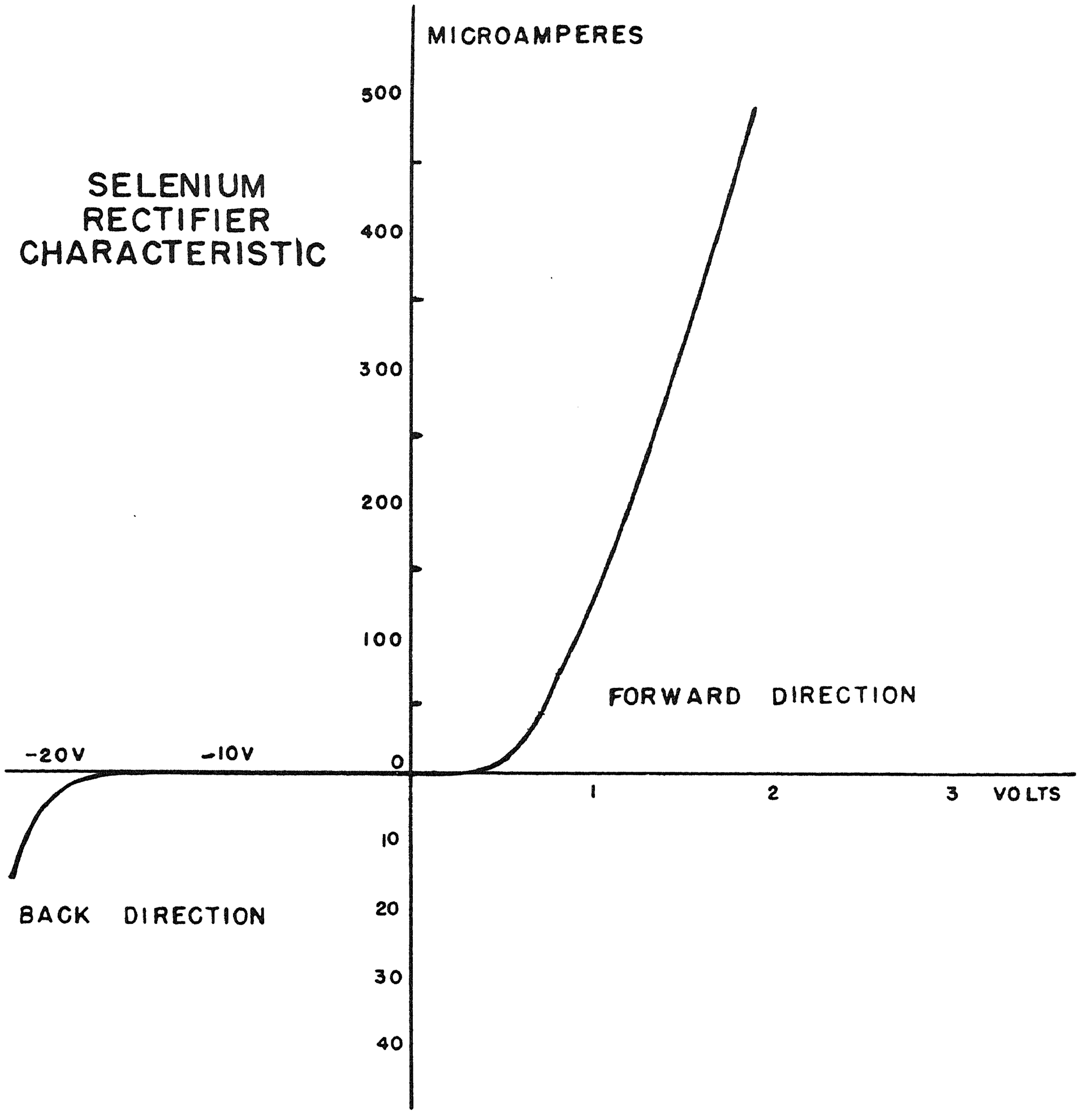

Fig. 1-2. Typical Rectifier Characteristic

Operating Conditions

The application of rectifier switching circuits is limited by the time constant of these circuits. This time constant is determined by the capacity of the rectifiers and by the current which the rectifiers are able to pass. The capacity of a selenium rectifier is directly proportional to its active area. This proportionality is true also for the back and the forward conductance of the rectifier. Hence it can be stated that the time constant of a selenium rectifier switching circuit is independent of the active area of the rectifiers used. The density of the current through the rectifiers will be the same in each case. As a consequence the use of rectifiers with a small active area will involve small currents. This is an important advantage in those cases where many rectifiers are fed from one current source. In the design of the Sequence Mechanism for Mark IV, for example, in some cases as many as 60 rectifiers are controlled by one cathode follower. A second advantage of small rectifiers is that a better path is available for the conduction of the heat generated in the active area. This permits the use of a larger current density. Finally, small rectifiers take less space and are less expensive than the larger types. The low cost per unit has decisively influenced the design of the circuits of Chapters 3 and 4.

The choice of the rectifiers used in the switching circuits to be described in the following pages has been limited to the types which are available commercially. The current and voltage values at which the rectifiers are operated have been determined from experience obtained in power circuits. With no previous experience available from the use of these rectifiers in switching circuits, a conservative choice was made. A forward current of 0.4 MA and a back voltage of 18 V has been used.

The cells were tested for a forward voltage of 1.8 V or less and for a back current of less than 20 Microamperes. The capacitance of these rectifiers is estimated at 70 $\mu\mu$F. The rectifiers have been used without forming. When formed, the back current at 18 V is less than one micro-ampere. The mounting of the rectifiers is illustrated by Fig. 1-3. It

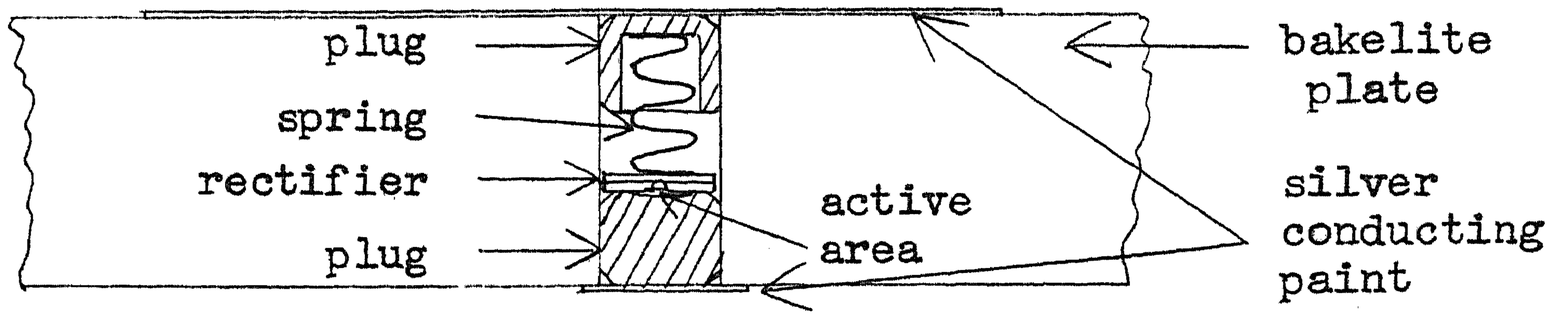

Fig. 1-3. Mounting of Selenium Rectifiers

should be noted that with this mode of construction the active area of the rectifier is not under pressure. This is of importance, since the characteristics of the rectifier become worse when pressure is applied.

Performance

The performance of the rectifiers, as used in the circuits which will be described in the following pages, has been very satisfactory. Several of these circuits have been in operation for eight months at the moment of this writing without failing or showing any noticeable changes in characteristics. The main cause for the failures that have occurred has been temporary overloading. This has occurred when a signal wire was shorted by mistake to a High voltage. The large current which flows through the rectifier in this situation develops an excessive amount of heat, which destroys the contact surface. The rectifiers have not shown any failure as a result of the high temperature of surrounding components. It can be observed that some rectifiers recover after overloading. This

may be due to the fact that a hole is burned in part of the rectifier surface. The hole represents an open circuit and the remaining part of the active area continues to function. If the active area is substantially reduced it is likely to be overloaded during the regular circuit operation and the circuit will fail after a short while. The experience has been that failures keep occurring for a period of about four days after the initial overloading occurred.

The total number of small rectifiers used in the Sequence and Slow Storage switching circuits is estimated at 5500.

B. Elementary Switching Circuits

Idealized Operation

The voltage-current curve of Fig. 1-2 can be simplified to the broken line of Fig. 1-4. This characteristic represents a circuit element

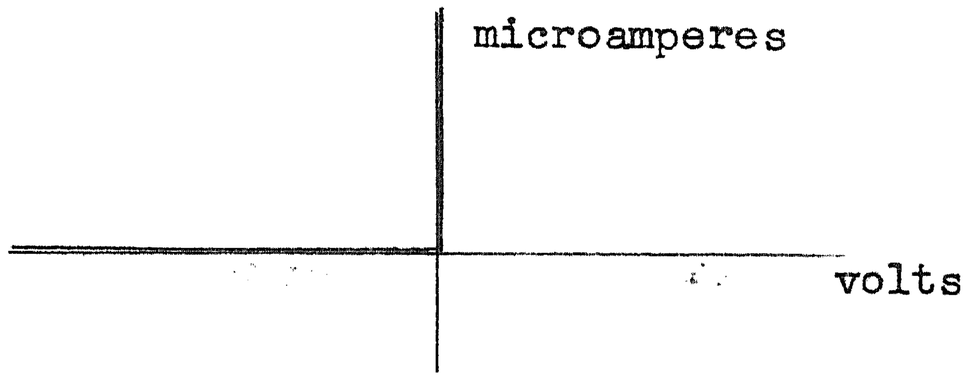

Fig. 1-4. Idealized Rectifier Characteristic

which has infinite resistance for a voltage applied in one direction and zero resistance for a voltage in the opposite direction. The switching circuits for selenium rectifiers will be discussed first on the basis of this simplified characteristic. This discussion will be followed by a consideration of the practical limitations which are imposed upon these circuits, due to the actual characteristics of the rectifiers.

Figure 1-5 shows a circuit in which the input signals $e_1,\ldots,e_n$

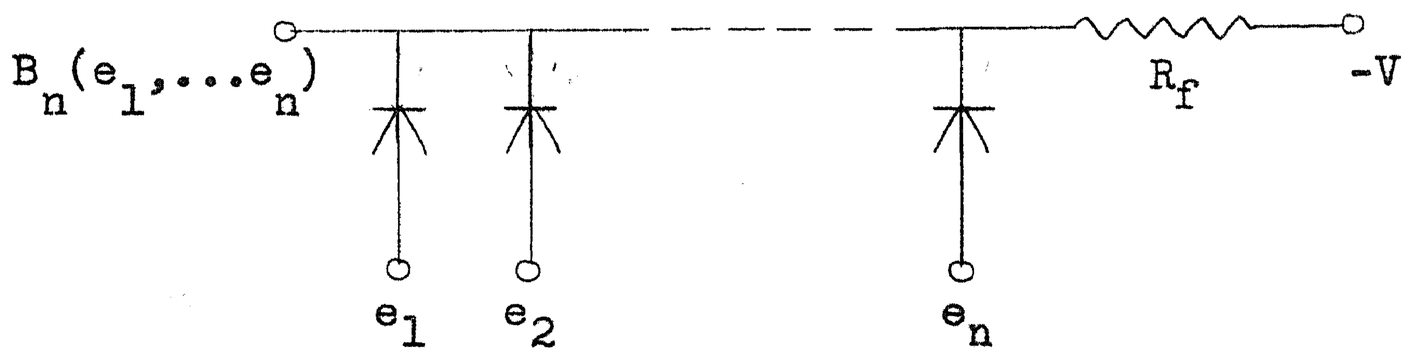

Fig. 1-5. Circuit for B_n

control an output signal B_n. Each of the input signals can have a positive value, which may be represented by the binary number 1, or a negative value, which may be represented by the binary number 0. The output B_n is a function

of the input signals and hence is written $B_n(e_1,\ldots,e_n)$. It can be seen from Fig. 1-5 that if one or more of the input signals has a high voltage the output voltage will be high also. A low voltage for the output will be obtained only when all input voltages are low. This can be expressed by the binary equation

$$B_n(e_1,\ldots,e_n) = 1 - \prod_{k=1}^{n} e_k',$$

where $e_k' = 1 - e_k$. By reversing the polarity of the rectifiers in the circuit of Fig. 1-5 the circuit of Fig. 1-6 is obtained. In this circuit the resistor is returned to a positive, rather than a negative, voltage. The output F_n for this circuit will be high only if all the inputs

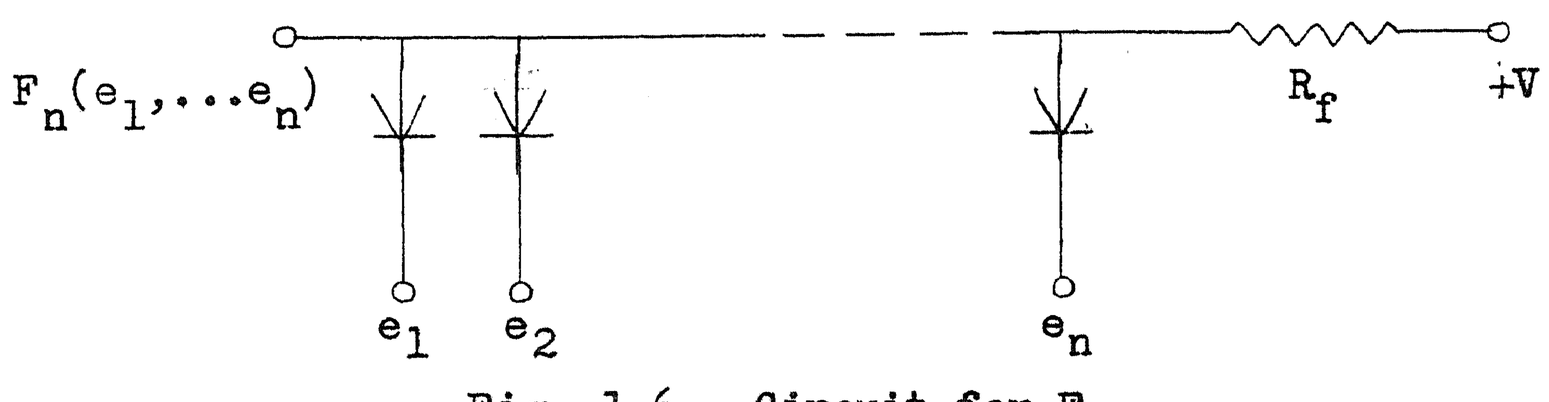

Fig. 1-6. Circuit for F_n

$e_1,\ldots,e_n$ are high. This can be expressed by the equation:

$$F_n(e_1,\ldots,e_n) = \prod_{k=1}^{n} e_k .$$

Since the ideal characteristic of Fig. 1-4 has been assumed for the rectifiers, the positive and negative voltages of the outputs will be equal to the positive and negative voltage values of the inputs. Hence, the outputs can be used in turn as inputs to other rectifier circuits. This is illustrated in Fig. 1-7. The output of this circuit can be described by the expression: $F_3(B_2,B_3,B_4)$. In a similar manner a circuit for $B_n(F_{k_1},\ldots,F_{k_n})$ can be constructed. The circuits for $B_n(B_{k_1},\ldots,B_{k_n})$ and

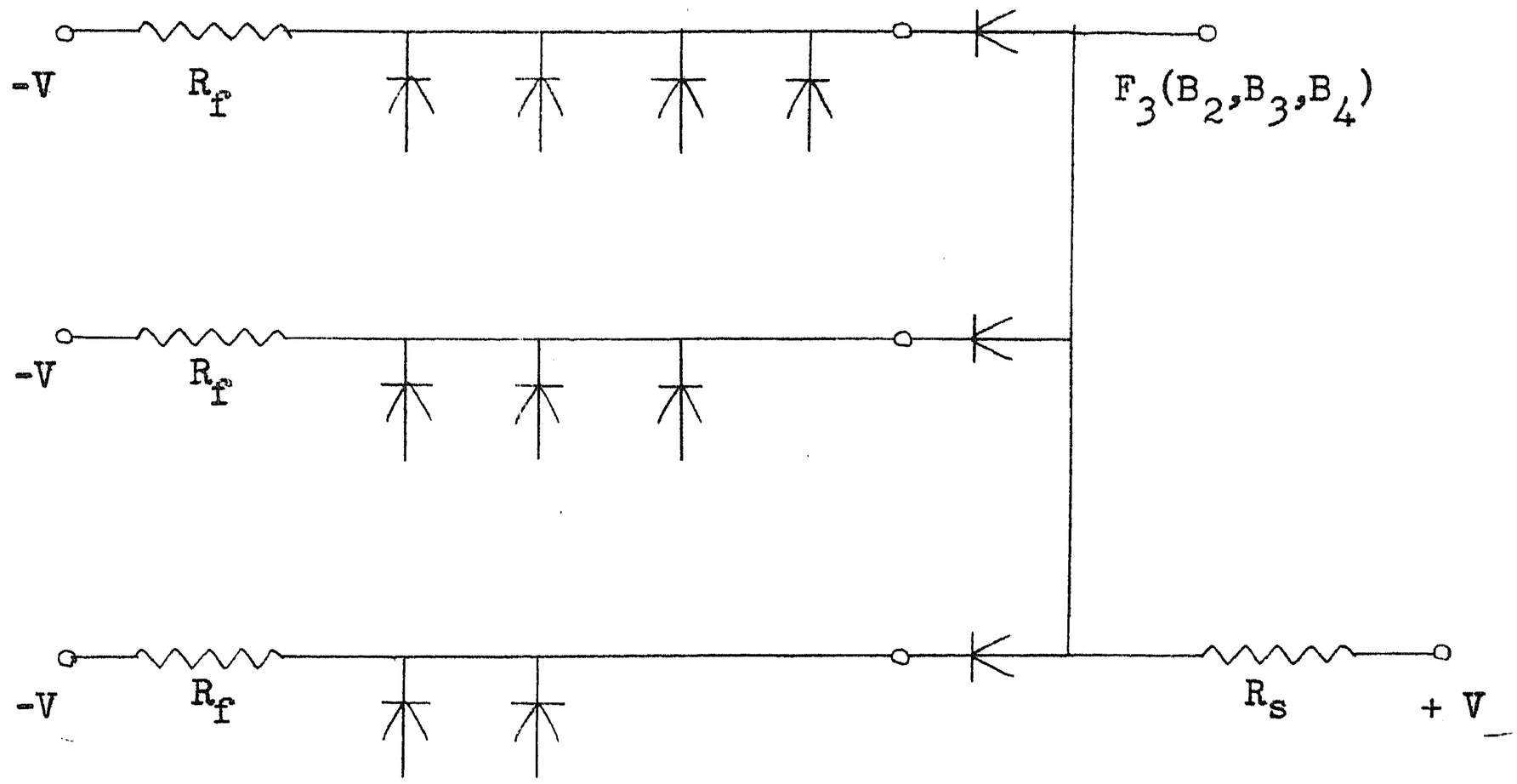

Fig. 1-7. Circuit for $F_3(B_2,B_3,B_4)$

$F_n(F_{k_1},\ldots,F_{k_n})$ are equivalent to the circuits for $B_{\Sigma k}$ and $F_{\Sigma k}$. This can be shown as follows:

$$B_n(B_{k_1},\ldots,B_{k_n}) = 1 - \prod_{j=k_1}^{k_n} B_j'$$

$$= 1 - \prod_{j=k_1}^{k_n} \prod_{i=1}^{j} e_1'$$

$$= B_{\Sigma k}$$

and

$$F_n(F_{k_1},\ldots,F_{k_n}) = \prod_{j=k_1}^{k_n} \prod_{i=1}^{j} e_i$$

$$= F_{\Sigma k}.$$

This leads to the conclusion that a new switching operator is obtained only in the case where the output B_n is used as an input to the circuit

F_k or vice versa. The resulting operator in turn is of the type B_n or F_n and can again be used as an input to a circuit of the type F_n or B_n respectively. This process can be continued to yield switching operators which are increasingly complex. Each operator of this kind can, however, be written in terms of the functions B_n and F_n. A further discussion of these operators is given in Synthesis of Electronic Computing and Control Circuits.[1] It is shown in this reference that any switching function can be represented by the expressions $B_n(F_{k_1},\ldots,F_{k_n})$ and $F_n(B_{k_1},\ldots,B_{k_n})$. Of particular interest also is the synthesis of rectifier switching circuits with the aid of Minimizing Charts, which is described in this reference.

In describing rectifier switching circuits it is convenient to introduce the term "level." The circuits of Figs. 1-5 and 1-6 are said to be single level circuits. They can be described with one of the functions B_n or F_n. A circuit of the type B_n which has as its inputs circuits of the type F_n can be described as a two-level circuit, with the operator B_n as its second level and the operators F_n as the first levels. Similar names can be given to a circuit for $F_n(B_{k_1},\ldots,B_{k_n})$ and more complicated functions.

In switching circuits which employ a large number of input sources the representation by means of the operators F_n and B_n tends to become too cumbersome. It has been found to be practical to use the terms "and" and "or" in such cases. These terms have the added advantage that they are more easily explained to maintenance personnel. They are used exclusively in the description of the circuits which is given in Chapters 3 and 4. The circuit of Fig. 1-5 will have a low output only if all inputs are low. The circuit thus can be considered an "and" circuit with respect to low signals. At the same time this circuit can be considered an "or" circuit with respect to high signals, since one or more high inputs will

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1. Staff of the Computation Laboratory, Synthesis of Electronic Computing and Control Circuits, Annals of the Computation Laboratory, 27, particularly Chapter X, Harvard University Press (1951).

result in a high output. Conversely the circuit for F_n (Fig. 1-6) can be described as an "or" circuit for low signals and an "and" circuit for high signals. Since it has been found convenient to describe circuits in terms of low signals, the first of the definitions mentioned will be used throughout the following chapters.

Practical Limitations

The application of the principles described above is limited by the degree to which the selenium rectifier approaches the ideal rectifier. Limiting factors are the power dissipation in the rectifier, the permissable back voltage and the capacity of the rectifier. In Part A of this chapter it was mentioned that a current of 0.4 MA and a corresponding voltage of 1.8 V has been chosen as the operating point on the forward characteristic of the rectifier. With these values the rectifier is operated well below its estimated power rating. The input signals to a rectifier circuit are almost without exception obtained from cathode followers. It can be seen from the voltage-current curve of Fig. 1-2 that the back current of the rectifier is still small at -18 V. With this voltage and current as the operating point on the back characteristic of the rectifier, the cathode resistors of the cathode followers should be returned to -15 V and the inputs to the cathode followers clamped at ground potential. Using one triode section of a 2C51 tube the cathode will have a positive voltage of 3 V with the grid grounded. The cathode follower will feed rectifier circuits which are either of the type B_n or F_n. The equivalent impedance of the load will be R_f/k, where R_f is the return resistance of the first level circuit and k the number of circuits fed by the cathode follower. This load impedance will be returned to a positive voltage in the case of

the circuit F_n and to a negative voltage in the case of the circuit B_n. As a result the negative output voltage of the cathode follower is less than 15 V in the case of F_n and more than 15 V in the case of B_n. Each of these cases becomes more pronounced when k is large. In the case of a B_n circuit no particular difficulty arises; in the case of a F_n circuit, however, the tolerance in the output signal of the rectifier circuit will be reduced. For this reason the circuit B_n has been chosen in most cases for the first level circuit. As a result the second level circuit, when present, is of the type F_n. It has been found that most of the conditions which are satisfied by rectifier circuits can be expressed in their simplest form by "and" conditions combined by one "or" condition. This would correspond to an "and" circuit in the first level and an "or" circuit in the second level. A first level of the type B_n can be considered an "and" circuit with respect to a low input and output. As a result most conditions are represented by a low signal rather than a high signal. A first level of the type B_n is also called a negative-sensing circuit; a circuit with first level of the type F_n is called a positive-sensing circuit. In the Slow Storage and Sequence system of Mark IV 313 negative sensing circuits and 13 positive sensing circuits are used. A negative sensing "and" circuit can also be used as a positive sensing "or" circuit. This is the case for the circuit SM described on page 4-70.

With a voltage swing of 18 V at the input of the rectifier circuit a negative return voltage of -45 V was chosen. This is a few times the input voltage variation. If the controlling input of a single level circuit changes from +3 V to -15 V the output will decrease exponentially. The limiting value of the exponential curve is -45 V. As soon as the output reaches -15 V the decrease will stop. As a result only the first,

steep, part of the exponential curve will be used. In the case of a two-level circuit a different situation arises, which is described below.

With one input of a first level high and all other inputs low the rectifier connected to the high input carries the current through the resistor and the back current through the back conducting rectifiers on that level. This latter current is usually neglected. However if one level is controlled by 10 or more rectifiers this current may be 0.2 MA or larger. In a case like this it may be worth while to use formed rectifiers. Circuits which require this many rectifiers per level do not occur very often. An example is the circuit of FSTP 11 (page 4-29) which uses a first level with 11 inputs. If the back current is neglected the first level resistor, R_f, can have a value of 110 K or larger, with a current through the rectifier of 0.4 MA or less. It is desirable to have a low resistance value in order to minimize the RC time delay.

For two-level circuits the second level resistor R_s is returned to +15 V. It is again desirable to have as low a value for this resistance as is possible. With all inputs to one first level at -15 V the second level output voltage is determined by the combination of first and second level resistance values. With a possible cut-off value of -5 V for the tube which is controlled by the second level output it was decided that the output of the selenium circuit should be -8 V or more negative. This determines the value of R_s. The current through the second level resistor contributes to the current through the first level resistor. As a result the resistance values of the first and second level resistors can be reduced. If the number of first levels is larger than two, the reduction in the resistance values becomes negligible . For a circuit with two first levels such as the circuit E20 (Fig. 4-87) an improvement can be achieved.

The speed of the rectifier circuits is limited by the capacitance which the rectifiers represent in the non-conducting state. In general the input to the circuit will be a square wave. The output of the rectifier circuit has a shape as is shown in Fig. 1-8b. This output is amplified

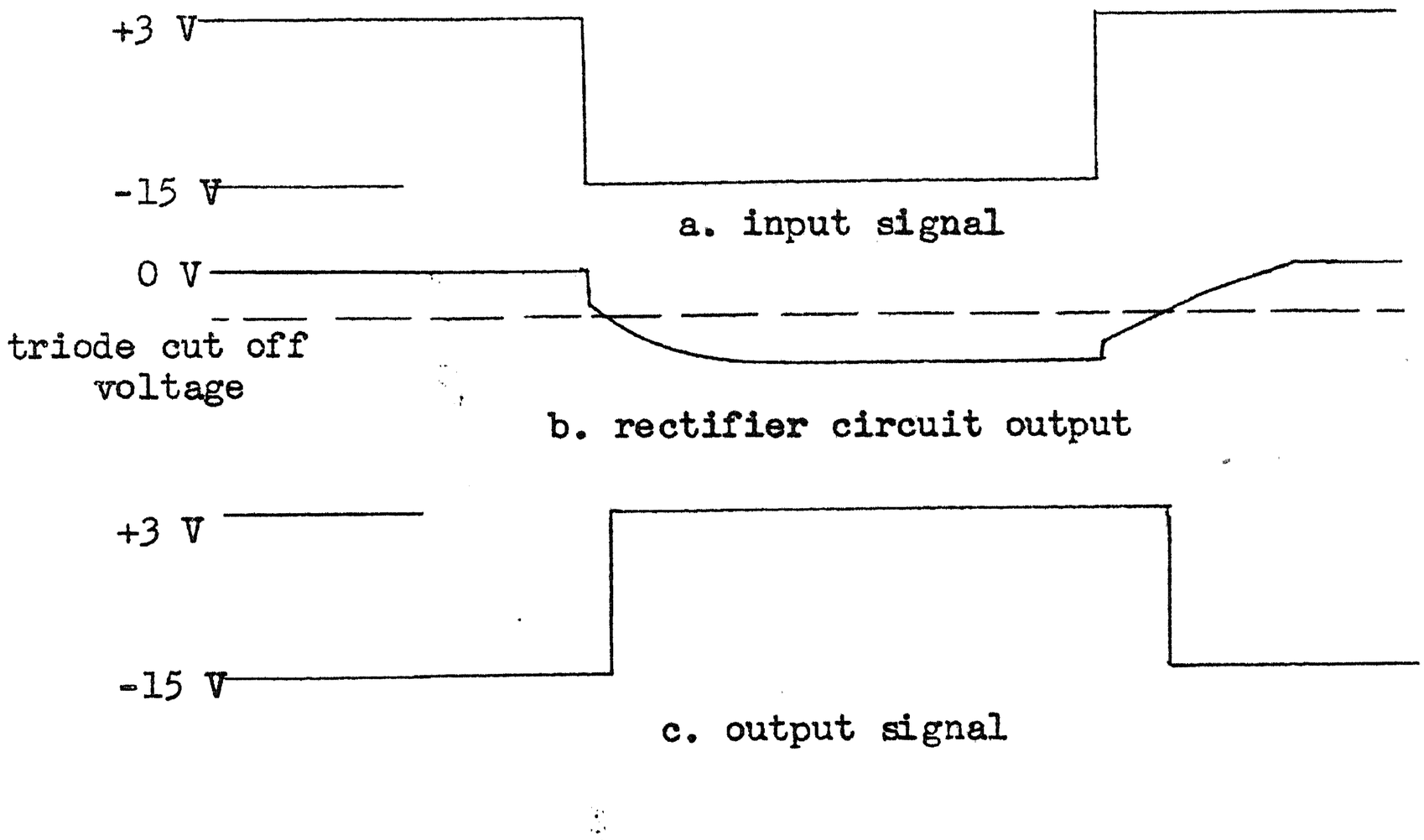


Fig. 1-8. Rectifier Circuit Input and Output Signals

and inverted in a d.c. amplifier and fed to a cathode follower. The output of the cathode follower in relation to the original square wave input (Fig. 1-8a) is shown in Fig. 1-8c. A time delay occurs in both the decay time and the rise time of the final signal. The cause of the time delay in both instances will be discussed for the general two-level circuit shown in Fig. 1-9. This circuit has n first levels and it will be assumed that n-1 of these first levels are high. Level 1 has m input rectifiers, controlled by the inputs $e_1,\ldots,e_m$. The signals $e_2,\ldots,e_m$ are assumed to be low. As a result of these assumptions the input e_1 will control the output of the circuit. The input signal is assumed to have a near square

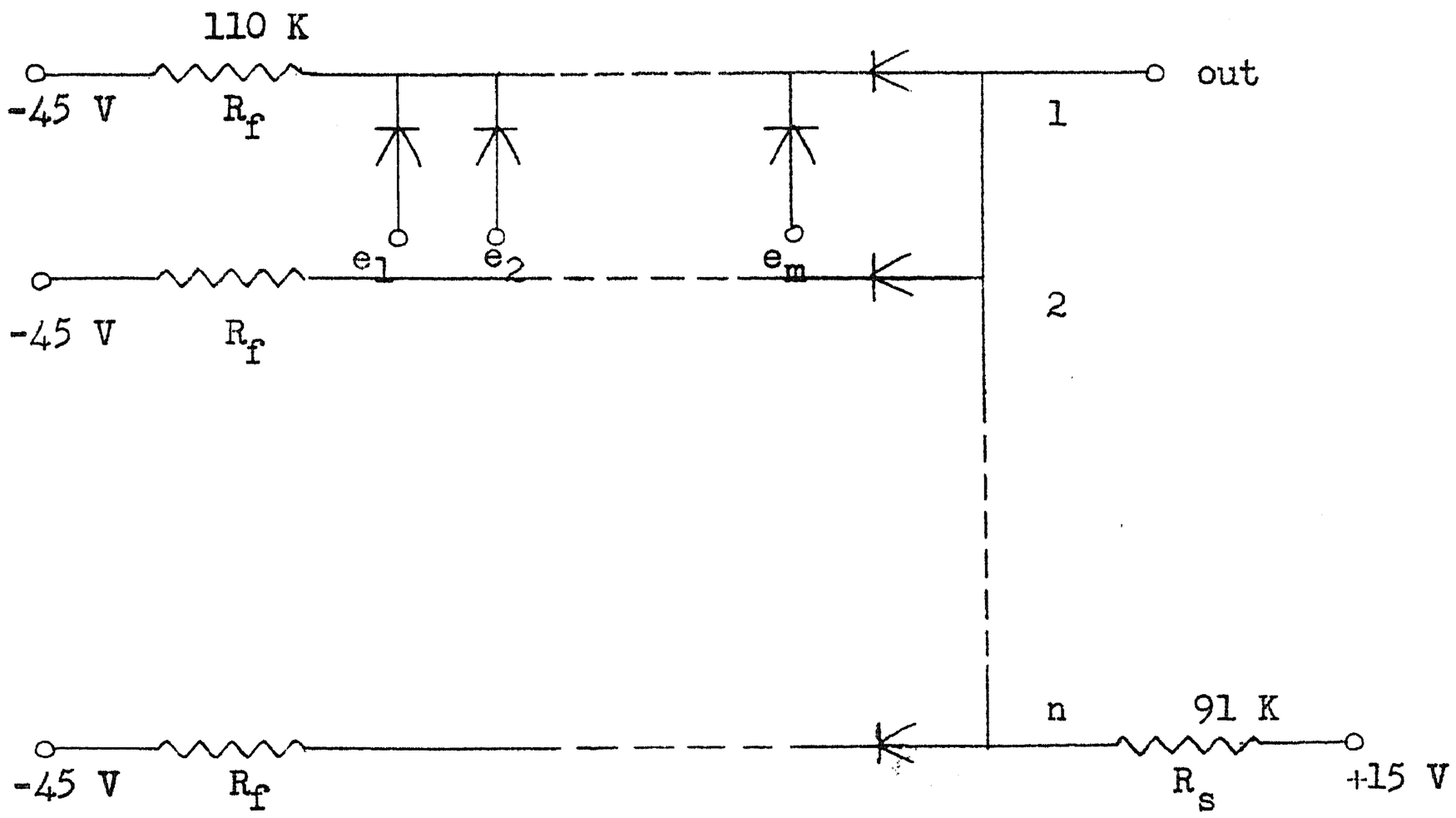


Fig. 1-9. General Two-Level Circuit

waveform, derived from a low impedance source, the cathode follower. When the signal e_1 changes from high to low the output voltage will become negative. Because of the capacitances which are in the circuit, the decay of the output voltage will be slow. Thus the rectifier which is controlled by e_1 will be in a back conducting state. The same is true for the other rectifiers on level 1 and for the rectifiers on the second level. In this state the rectifiers have a high resistance and their capacitance becomes predominant. This situation is illustrated in Fig. 1-10 where the rectifiers which are involved in the operation have been replaced by their capacitance. The time constant, which expresses the speed of the circuit, is determined from the sum of the rectifier capacities C and the resistors of first and second level in parallel. Thus the time constant for decay, T_d, becomes:

$$T_d = \frac{R_s R_f}{R_s + R_f} \cdot (n+m)C \ .$$

The fact that the decay curve as shown in Fig. 1-8 is not a purely exponential

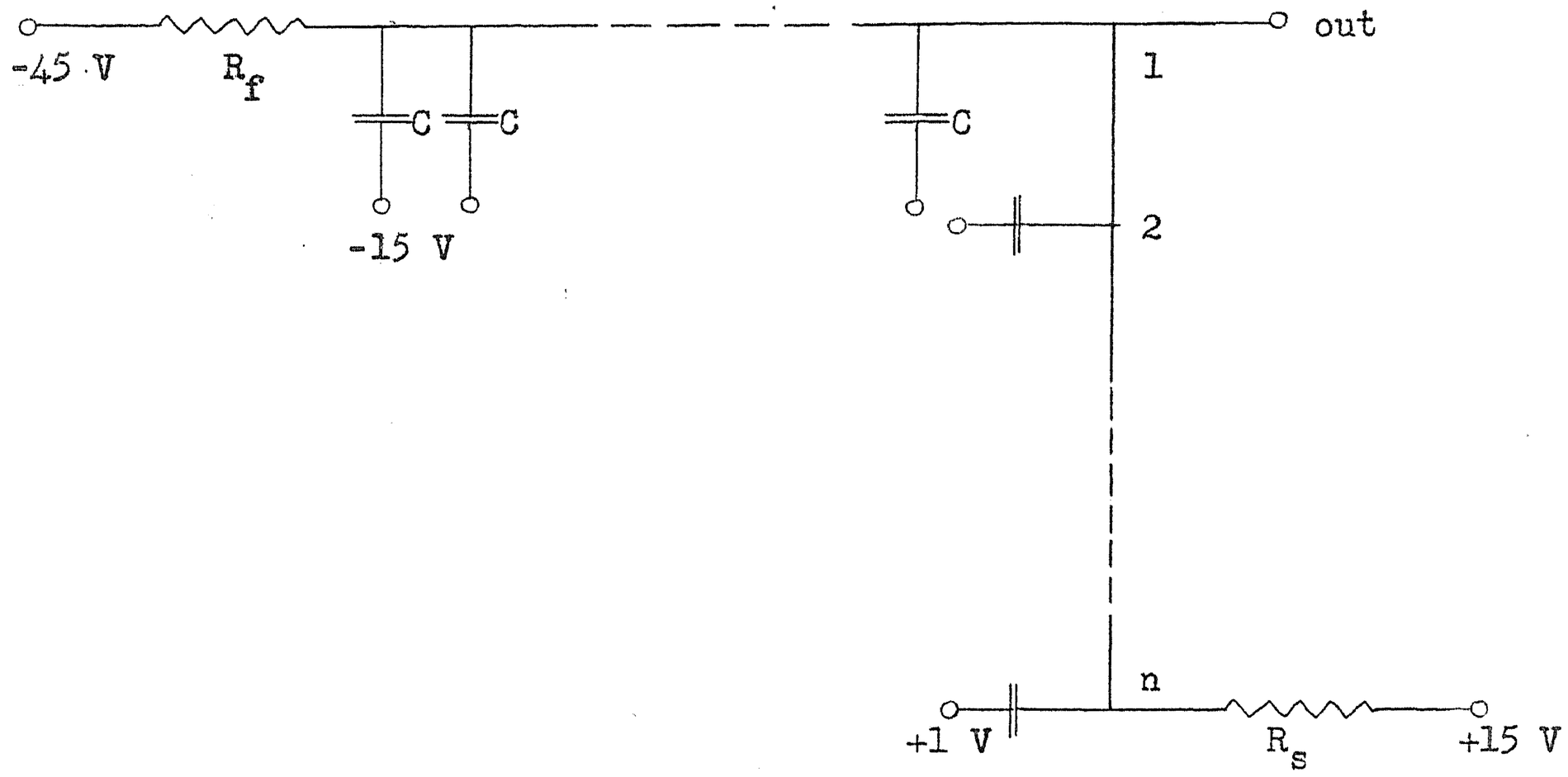


Fig. 1-10. Equivalent Circuit for Decay Time

curve is explained by the non-linear characteristic of the rectifiers. During the first part of the decay the rectifier connected to e_1 is still conducting and as a result the low impedance of the cathode follower is in parallel with R_f and R_s. Thus the first part of the decay is rapid, followed by a slow decay as soon as the controlling rectifier stops conducting in the forward direction. The output of the selenium rectifier circuit is connected to an amplifier with grounded cathode. The grid current of the amplifier tube will prevent the output from going more positive than part of a volt. When the output of the circuit becomes less than the cut-off value of the amplifier, the tube stops conducting and the amplifier output changes from a low voltage value to a high value. All selenium circuits have been used with 2051 double triodes, which have a cut-off voltage of from 3 V to 5 V with 100 V at the plate. This cut-off value is shown in the curve of Fig. 1-8b. It can be seen that the tube is cut off just after the fast decay changes to the slow decay. As a result the decay time is greatly reduced by the fast initial decay.

In the transition from a low to a high value of the input e_1, the first level circuit acts independently of the second level circuit. The situation which prevails is shown in Fig. 1-11. The rectifier which

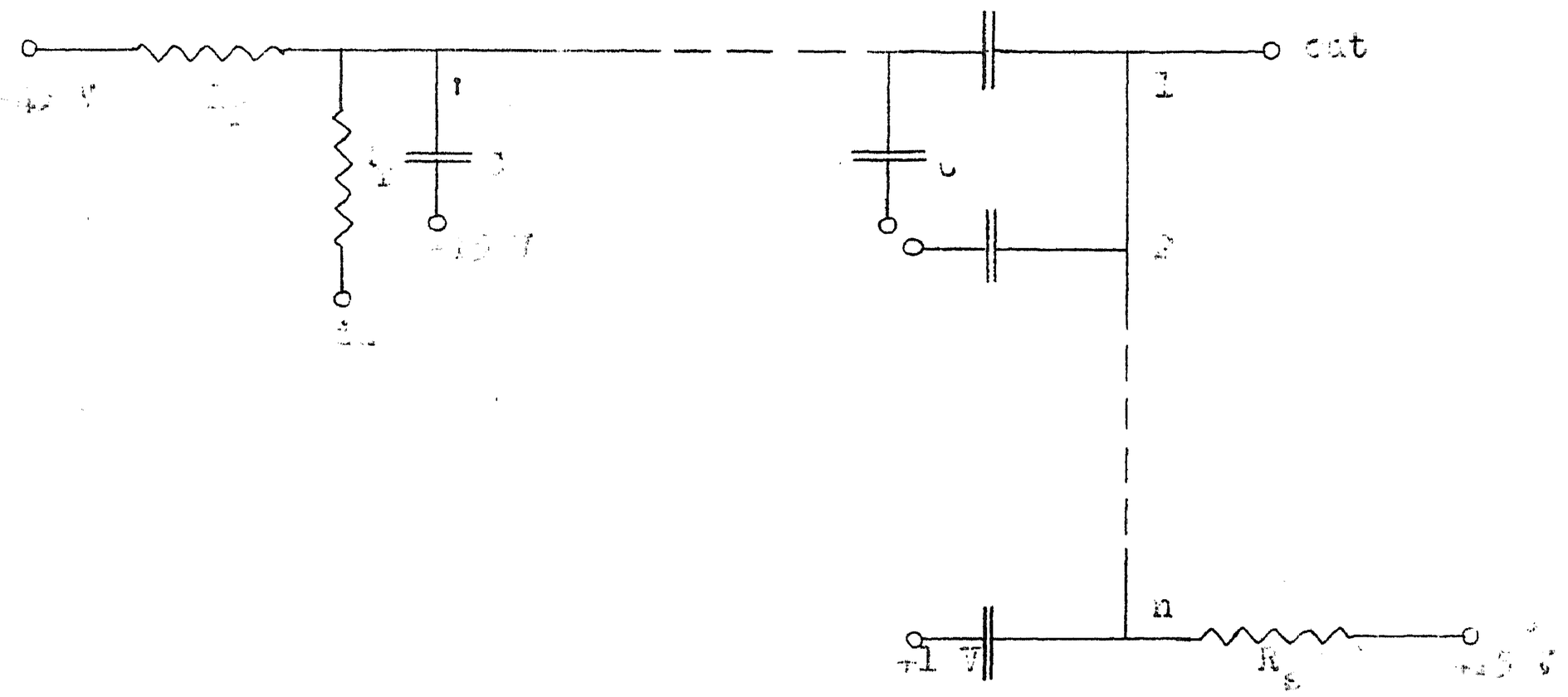


Fig. 1-11. Equivalent Circuit for Rise Time

is connected to e_1 is conducting in the forward direction and is represented by the resistance R_f. This resistance and the low impedance of the cathode follower, R_c, are now in parallel with R_f and will enable the capacitances of the first level rectifiers to be charged rapidly. The time constant for the first level rise, T_{rf}, is:

$$T_{rf} = \frac{R_f(R_c+R_r)}{R_f+R_c+R_r} \cdot m \cdot C .$$

As soon as the voltage of the first level becomes positive with respect to the second level voltage the input rectifier to the second level will be in a back conducting state. It is represented in Fig. 1-11 by its capacitance, C. The n rectifier capacitances in the second level will be charged through the second level return resistor R_s. The time constant for second level rise, T_{rs}, is:

$$T_{rs} = R_s \cdot n \cdot C .$$

This time constant controls the rise time of the rectifier circuit. Again, as was the case for the decay curve, the curve which can be observed for the rise of the circuit is not of the simple exponential character. Because the input rectifier to the second level is initially conducting in the forward direction the second level will rise sharply in the beginning. Once the rectifier is conducting in the back direction it is equivalent to a condensor. During the second period of the rise time the second level capacitances will be charged through the return resistor R_s only. Finally the connecting rectifier becomes conducting in the forward direction again. It can be seen from Fig. 1-8 that the cut-off value of the amplifier tube is passed on the flat part of the rise curve. This part of the curve is well described by the formula for T_{rs}. From the above discussion it can be concluded that the decay time of a two-level rectifier circuit is shorter than the rise time and that the latter is to a great degree dependent upon the value of the second level return resistor R_s, the capacitance of the rectifiers C and the number of first levels n.

The current through the rectifiers of the second level is considerably smaller than the current through the first level rectifiers. An improvement of the circuit might be achieved by using smaller rectifiers in the second level than in the first level. This method has not been employed, however, in the design of the circuits for Mark IV which are described in Chapters 3 and 4.

The analysis for the two-level circuit can be extended to three-level circuits and circuits with more levels. The solid and dashed lines of Fig. 1-12 show a three-level circuit. The third level, which is an "and" circuit, has two inputs. In this circuit the decay time of the output is determined by the third level return resistor R_t and the number

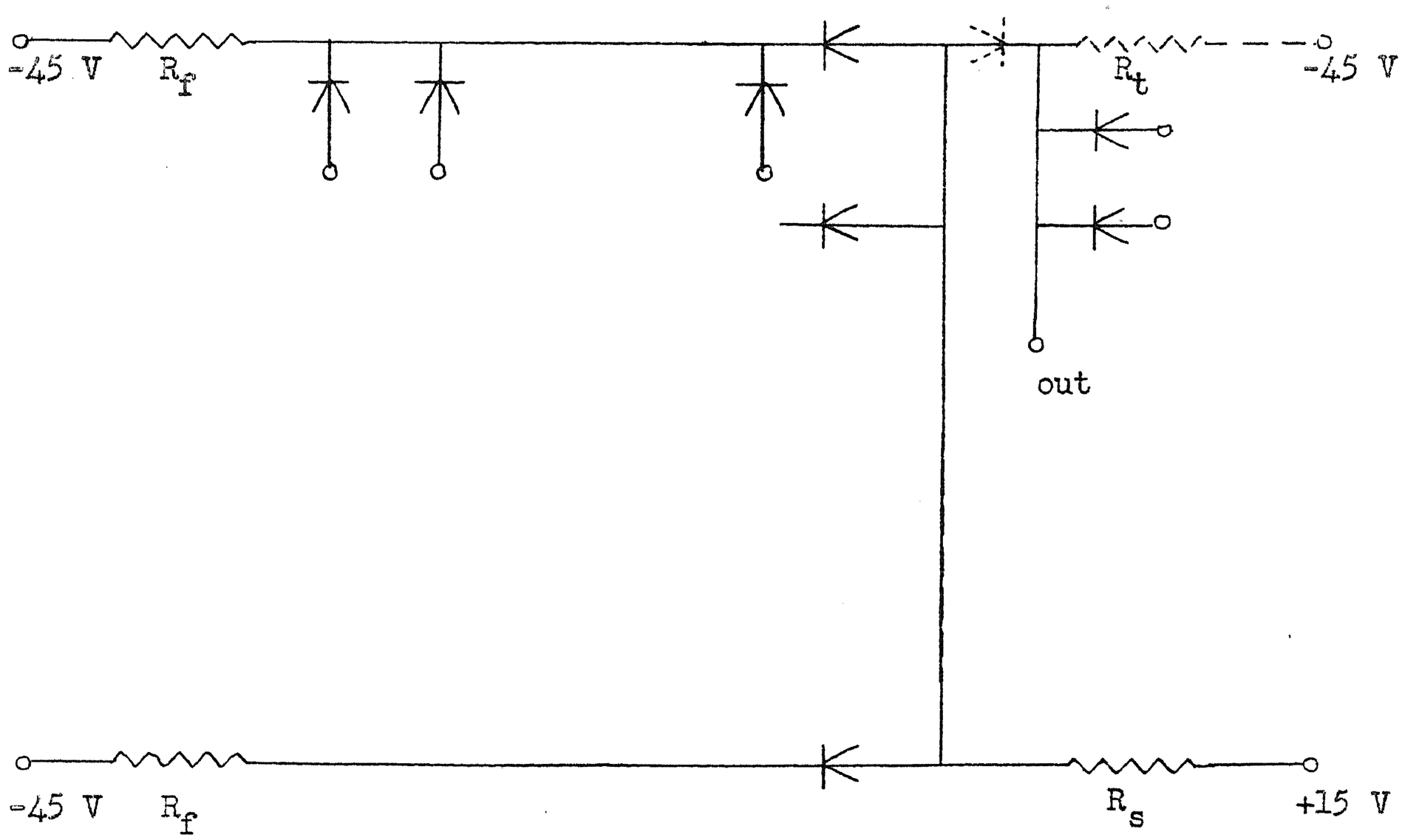


Fig. 1-12. Three-Level Circuit

of inputs to this third level. The value of R_t should be such that the voltage divider formed by R_s and R_t gives a positive output. If R_t is returned to -45 V, it should have a resistance value of at least three times the value of R_s. Thus the third level resistor is considerably larger than the second level resistor, causing the circuit to operate slowly. If this analysis is continued to circuits with even more levels it can be shown that each time the number of levels is increased the speed of the circuit is drastically reduced. This is one of the reasons why circuits with more than two levels are undesirable. A second reason is that for circuits of this nature the number of rectifiers involved tends to become large. In the design of the Sequence and Storage system of Mark IV one- and two-level circuits were used exclusively. In total 19 one-level circuits and 309 two-level circuits were used. In a few cases signals were combined

in an auxiliary circuit, the output of which was fed to several other circuits. The use of the auxiliary circuit might have been eliminated by the use of three- and four-level circuits. The reduction in the number of rectifiers and the simplicity of the overall design made the first choice by far more desirable.

The three-level circuit shown in Fig. 1-12 can be used to illustrate an alternate solution. If the third level resistor and the output rectifier of the two-level circuit are omitted, a simplified three-level circuit is obtained. The output of this circuit can be low only if the third level rectifiers have a low input. With a high input to one or more of the third level rectifiers the output will be high at all times. The current through these rectifiers will hold all first levels high. This means that this current may be several times 0.4 MA. This restricts the use of this method to those cases where only one first level can be low at a time. The circuit of Fig. 4-89 illustrates the use of this kind of third-level control. The desirability of a low value for the resistors used in a selenium rectifier circuit limits in a similar way the use of a single first level as an input to two or more second level circuits.

The rise time of a two-level rectifier circuit is approximately proportional to the number n of second level rectifiers as has been mentioned previously. This number can be reduced by means of a "whiffletree" circuit as is shown in Fig. 1-13. This figure shows a circuit with five first levels. These are grouped in a group of two and a group of three and connected through a series rectifier to the second level. If the output is controlled through a rectifier on level 1 the capacitance of the second level is no longer 5C, but $(\frac{2}{3} + \frac{3}{4})C$, or less than 2C. This is a substantial improvement and has been applied to all circuits having more than three

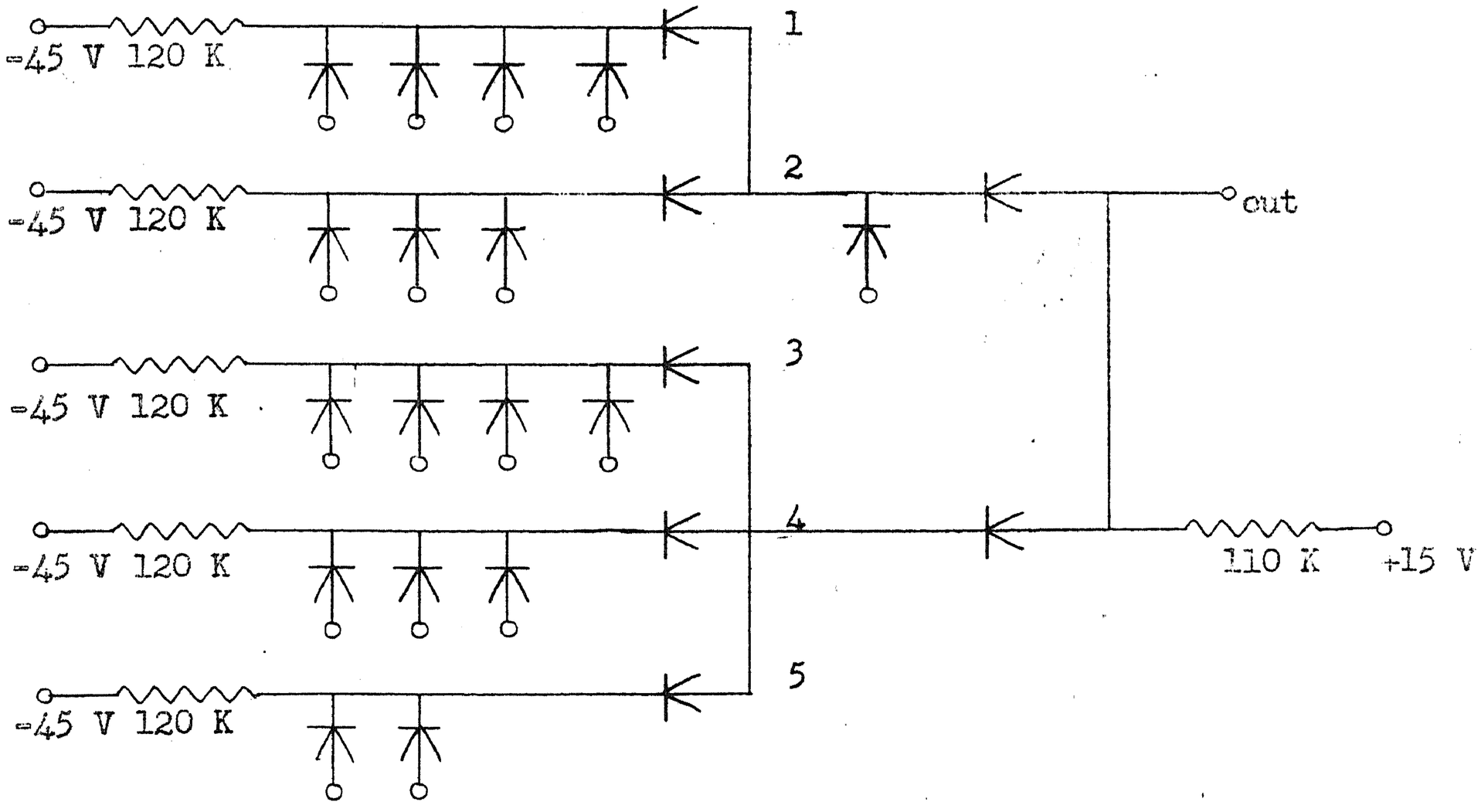


Fig. 1-13. "Whiffletree" Circuit

first levels. The schematic diagram of Fig. 1-13 is equivalent to the circuit for E3 which is shown in Fig. 4-79. The diagram also shows the use of a common control rectifier for the first levels 1 and 2. The use of this kind of common rectifier is subject to the same limitations as have been described for the circuit of Fig. 1-12. Figure 4-85 shows a circuit for twenty first levels, which have been grouped in groups of four and five. The circuit has a rise time of 6 microseconds. This is the average rise time for the circuits of Chapters 3 and 4. Circuits having as many as twenty-five first levels have been used. If desired even larger numbers of first levels can be used.

The method of grouping rectifiers could be applied also to the first level rectifiers. It has been pointed out, however, that the number of first level rectifiers does not greatly affect the speed of the circuit.

This has been confirmed by experiments. A disadvantage of grouping first level rectifiers is the added drop in the first level output and, as a result, in the final output of the circuit. The voltage drop for one rectifier is 1.8 V or less. With an input voltage of +3 V the output of the second level will be 1.5 V or higher. A voltage of at least 1.5 V is desirable in order to have the amplifier tube fully conducting. With two or more rectifiers in series in the first level the output will be about 0 V or less, which is too low. It can be verified that the addition of extra rectifiers in the second level tends to raise the output and thus improves the circuit. If necessary the output of the selenium circuit can be raised by substituting a voltage divider for the second level resistance and using the center tap as output. This, however, reduces the tolerance for the low output of the circuit and increases the number of circuit elements. This type of circuit has not been applied in the Sequence and Storage design.

Basic Switching Unit

In the previous section the limitations which govern the design of a selenium switching circuit have been mentioned. It was found that the most desirable circuit is a one- or two-level circuit representing an "and" condition in the first level and an "or" condition in the second level. It has been shown also that the output signal of such a circuit is different from the input signals. This difference is two-fold: a) The output signal differs in its waveshape and voltage levels from the input signal as illustrated in Fig. 1-8. b) The output signal is a high impedance signal in contrast to the low impedance signal supplied by the input cathode followers. These two limitations make it impossible to use an

output signal of one selenium rectifier circuit to control another circuit of the same kind. The selenium circuit alone is consequently incomplete as a switching element. In order to make the circuit complete in this sense, both a voltage amplifier and a power amplifier have to be added. These functions are performed by the d.c. amplifier and the cathode follower which have been mentioned previously. The amplifier also reshapes the output signal so as to provide a square final output signal. Figure 1-14 shows

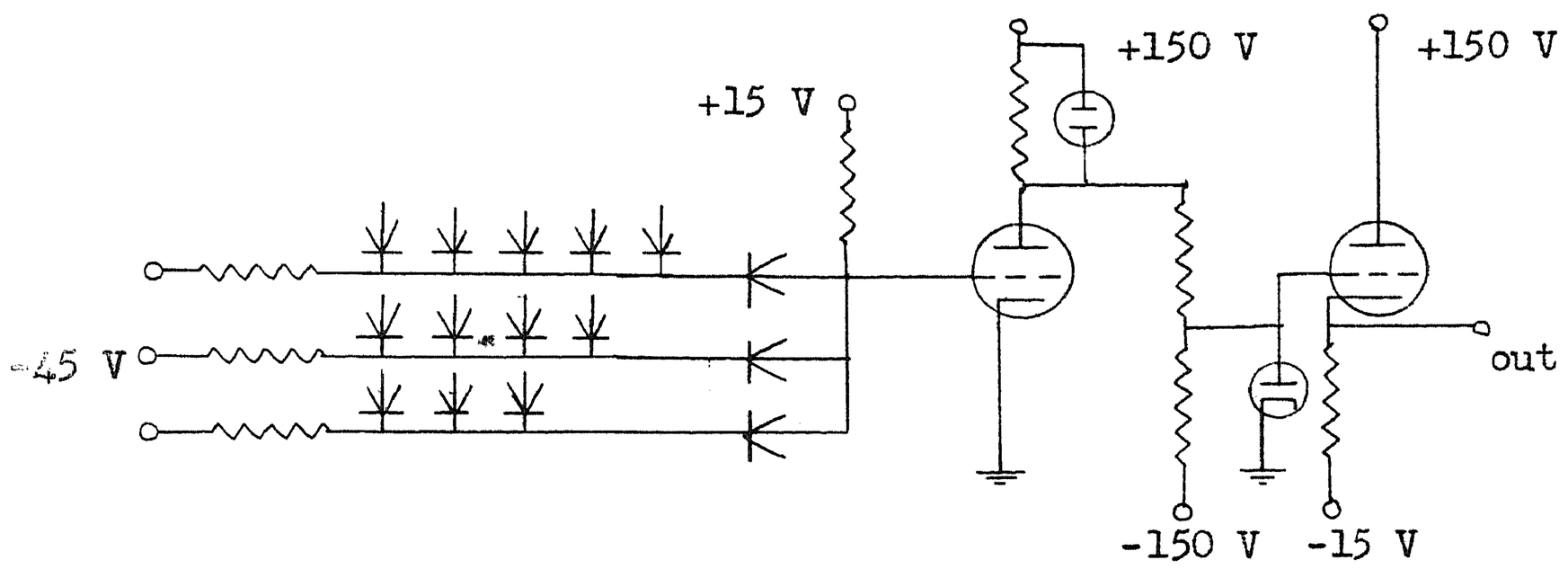


Fig. 1-14. Rectifier Circuit with Output Tubes

a selenium circuit with amplifier and cathode follower. The output of the amplifier varies between +8 V, when cut off, and -35 V when fully conducting. The output of the cathode follower is limited by the return voltage of -15 V and the diode clamper to ground. A neon light can be added conveniently in the plate circuit of the amplifier. Figure 1-15a shows a schematic representation of the circuit of Fig. 1-14. This kind of representation is used throughout Chapters 3 and 4. The selenium circuits differ only in the number of first levels and the number of rectifiers at each level. The triode amplifier of the unit is represented by the circle marked T_1, the cathode follower is represended by the circle marked C_1. With a low output of the selenium rectifier circuit the output

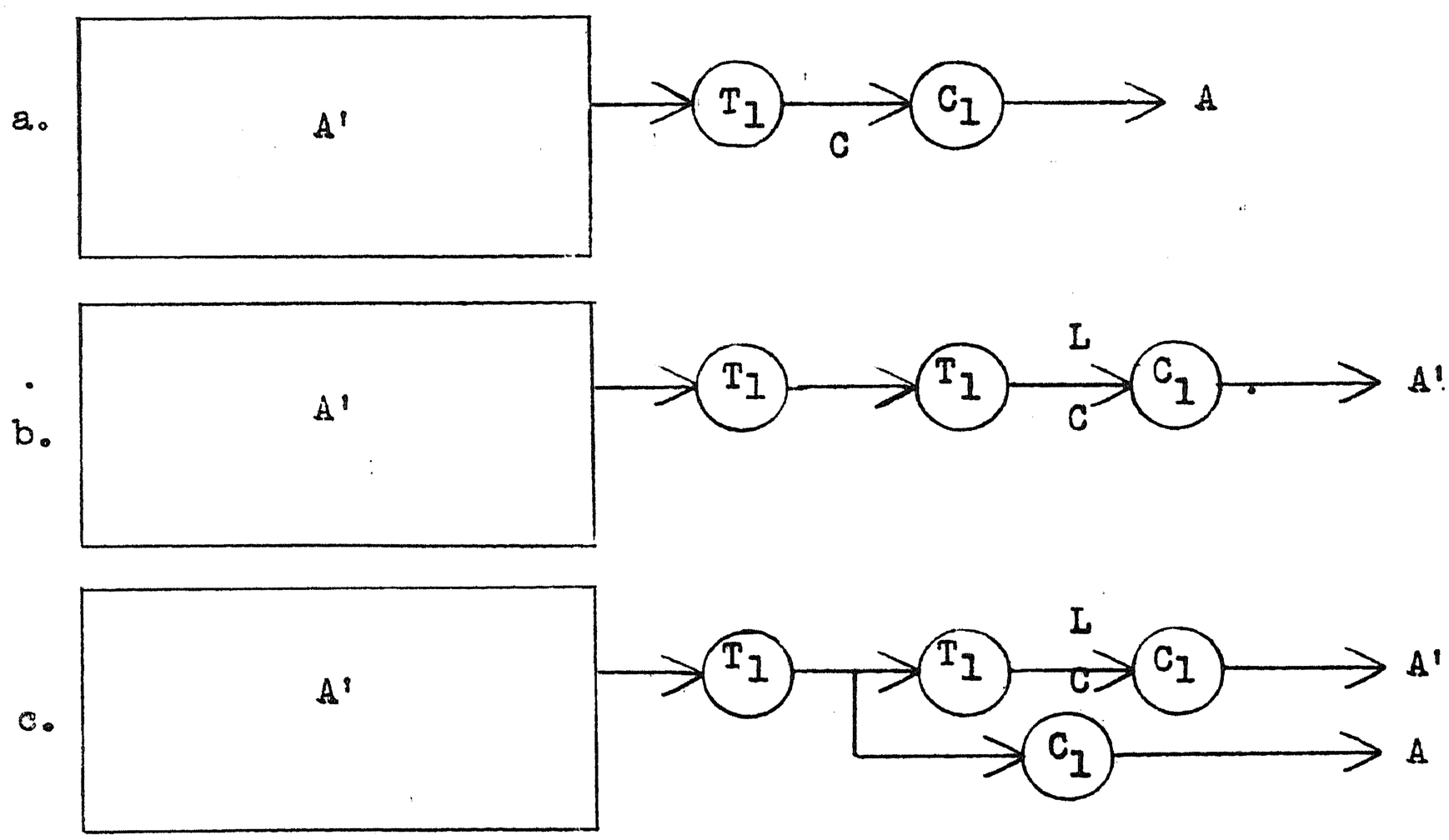


Fig. 1-15. Basic Rectifier Switching Units

of the cathode follower of Fig. 1-15a is high. In many cases a low instead of a high output is desired. This can be obtained by adding one inverter, as is shown in Fig. 1-15b. The letter L indicates that the neon light is placed in the plate circuit of the second amplifier. The light will be on when the output of the rectifier circuit is low and as a result the final output is low. The letter C indicates the presence of a clamping tube. In case both a high and a low output are desired, the circuit of Fig. 1-15c can be used. The circuits of Fig. 1-15 can be described as two-, three- and four-grid circuits. The rectifier circuits have been constructed using the mounting shown in Fig. 1-3. The connections between rectifiers are made with conducting paint. A rectifier circuit is at times referred to as a "card." It is possible to connect cards together to form a single switching circuit. This has been explained in Chapter 4.

For the circuits described in Chapters 3 and 4 a total of 12 types of general rectifier cards have been necessary. In addition 8 types of special purpose rectifier cards have been designed. The latter type of cards is used in one or two places only. Various types of rectifier cards are shown at the end of Chapter 4.

The above considerations concerning the basic switching unit apply to those circuits which are intended to control other rectifier circuits. From this point of view a circuit like the Sequence Unit of Mark IV can be considered as one large rectifier matrix. The cross-over points of this matrix are located in the rectifier cards, where the wires are combined. The final output of the card in turn controls a wire of this matrix. In this way each wire of the matrix is derived from a cathode follower which in turn is controlled by the other wires of the system. Various feed-back loops may exist in the system. This will be discussed more fully in the following part. The above picture is not complete, however, without including the signals which are introduced from the outside to control the circuit and the signals which are produced in order to control other units. In the following paragraph a few methods of control which are suitable for use with switches and relays are mentioned.

A switch can be used to replace a rectifier, because its operation is equivalent to the operation of the ideal rectifier. Figure 1-16 shows

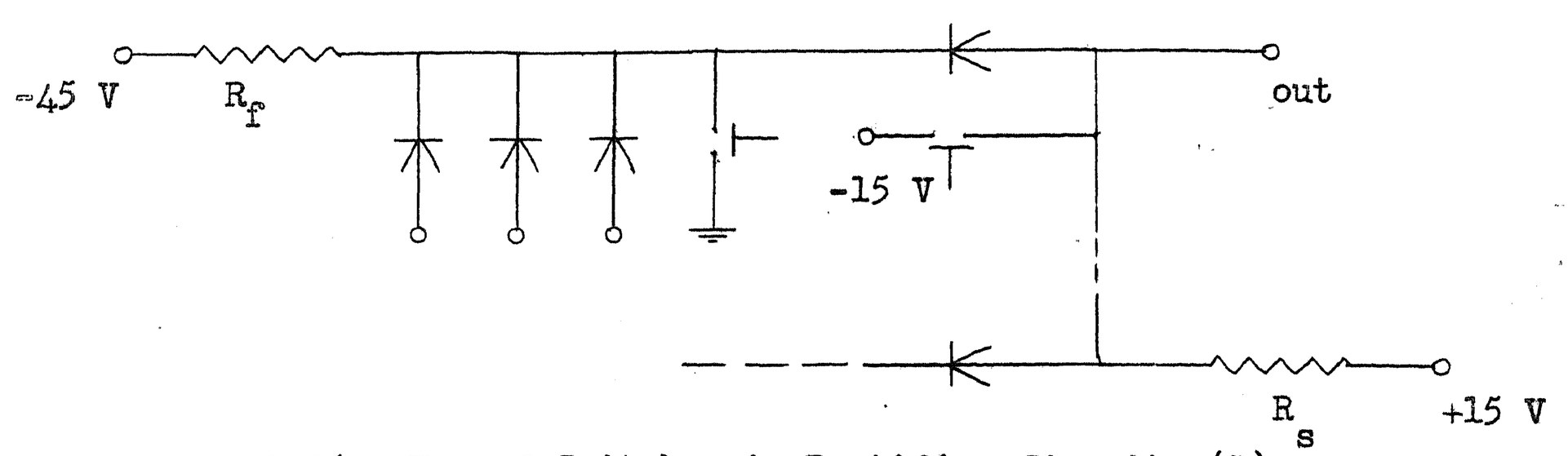


Fig. 1-16. Use of Switches in Rectifier Circuits (1)

the use of a switch in an "and" and in an "or" circuit. The first method has been used in the circuit for SM as described in Chapter 4, page 4-70. The rectifier card used is shown in Fig. 4-83. A disadvantage of this method is that the switching is performed in the high impedance part of the circuit. This is of importance when long wires are necessary to connect the switch to the rectifier circuit. An alternate method is shown in Fig. 1-17. This circuit makes use of the fact that a first

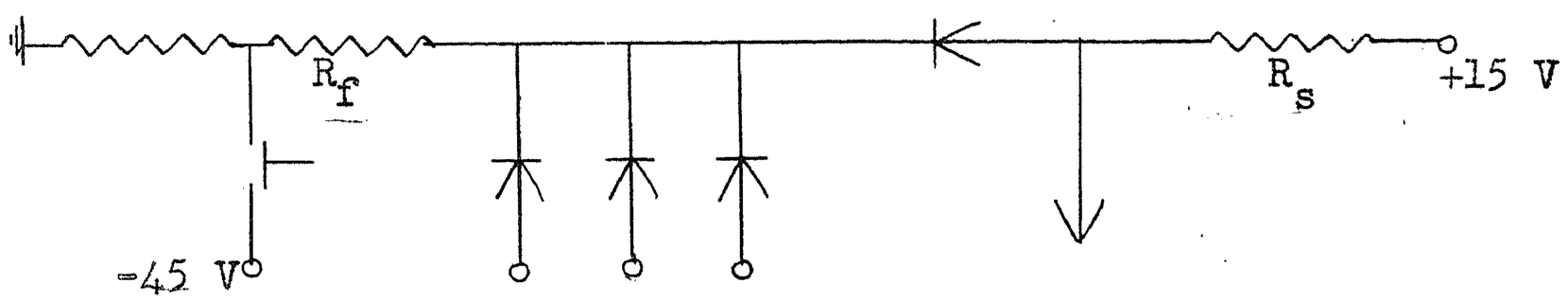


Fig. 1-17. Use of Switches in Rectifier Circuits (2)

level is inoperative unless its resistor is connected to a sufficiently negative voltage. The operation performed by the switch in this circuit is again equivalent to the switching function of a rectifier. This method has been used widely with relays and switches. Applications are shown in Chapters 3 and 4. A third method is to feed a control signal through a relay contact, as is illustrated by the signal Y DT' described on page 4-56.

A rectifier circuit in turn can be used to control relays, step switches and indicator lights. This can be obtained by placing the desired coil or light in the plate circuit of the amplifier which is controlled by the rectifier circuit. Chapter 3, page 3-12, describes a circuit in which the first level return voltage is controlled by a cathode follower with large swing. In the same chapter an application can be found of the switching of short pulses by means of selenium rectifier cards. The pulses are obtained from static magnetic delay lines and are switched with a

standard rectifier circuit of the type E20 (Fig. 4-87). The duration of the pulses is about 6 microseconds. With a decay time which is shorter than the rise time the output pulse is wider than the input pulse. Finally it may be remarked that in some cases it may be convenient to replace the triode amplifier by a pentode, double triode or other vacuum-tube operator. The use of a pentode is shown in Fig. 4-88, the use of a double triode is illustrated by the circuit for M-3 (Fig. 4-9).

CHAPTER 2

MULTIPLE STATE SWITCHING CIRCUITS

A. Multiple State Circuits

In Chapter 1 a selenium rectifier switching circuit has been described, which combines several input signals to produce a single output signal. It was pointed out that the way in which the signals are combined can most frequently be described as a number of "and" conditions combined by one "or" condition. Circuits of various size are used to represent conditions which are desired. When one or more switching circuits are controlled by one set of input signals, the operation performed can be described as a translation. To each configuration of the input signals belongs a set of output signals, which can be considered as the translation of the input signals. It is possible in this way to change from one coded number system to another or to perform the transformations necessary for an addition or multiplication. The circuits used in the Accumulator, the Multiply Unit and the Divide Unit of Mark IV are based on this principle. Several applications of such translation circuits are shown in Chapters 3 and 4.

It has been established in the previous chapter that a basic rectifier switching unit consists of a rectifier circuit together with an amplifier and cathode follower. The output of such a circuit can in turn be used as an input to other rectifier circuits. In the following pages various circuits will be discussed in which the output is used as an input to the circuit itself. In this way a feedback loop is established which permits these circuits to have two or more stable states. This kind of circuit is called a multiple state circuit. The state of such a circuit can be changed under control of external signals. A condition which

causes a change of state may involve several "and" and "or" requirements and thus require a large number of rectifiers per level or a large number of first levels for the switching circuits. In the following discussions each condition of this sort will be represented by a single input. This does not affect the principle of the operation of the circuits.

In representing the conditions for a rectifier circuit a method is used in which the input signals which control one first level are listed on a horizontal line. Each first level is listed on a separate line together with the name which describes the function of the level and the number of the level. This method of representation is used throughout Chapters 3 and 4, and is discussed in greater detail on page 4-2.

Trigger Pairs

The circuit of Fig. 2-1 has been derived from the circuit shown

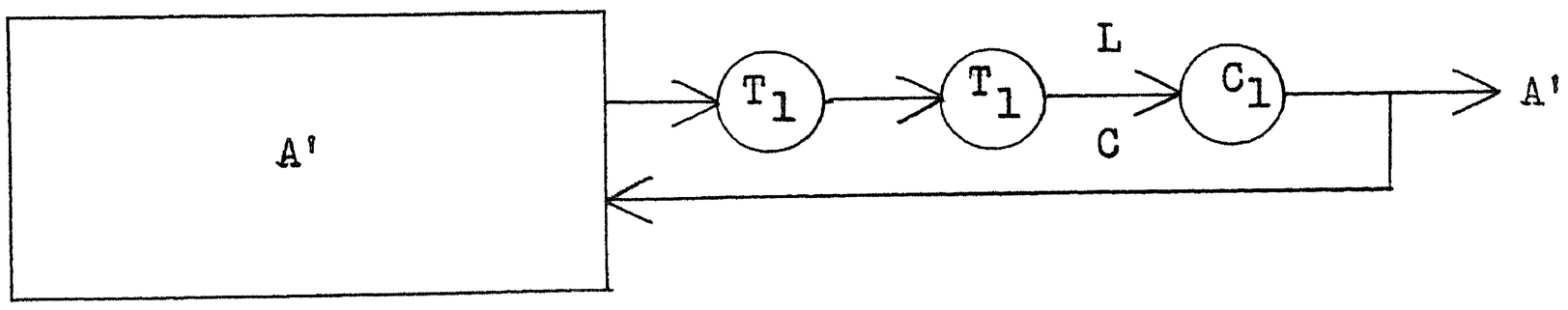


Fig. 2-1. Three-Grid Trigger Pair

in Fig. 1-15b by the addition of a feedback loop. The output signal A' will be low for any condition which makes one or more of the first levels of the rectifier circuit low. This output A' has in turn been used as an input to one of the first levels, commonly called the hold level, of the rectifier circuit. The conditions for A' are listed in Fig. 2-2. Level 1

1. hold	A'; reset
2. read-in	read-in

Fig. 2-2. Conditions for a Three-Grid Trigger Pair

is the hold level and has as inputs A' and a normally low reset signal. Level 2 has been called the read-in level and is controlled by a normally high read-in signal. With the reset and read-in signals in their normal state, the output A' can be either high or low. A high output A' will cause the hold level to be high and with the read-in level normally high, the output of the rectifier circuit will be high. This high output is consistent with the high output of the cathode follower. As a result the circuit will remain in this state. If, however, the output A' is low, the hold level will be low and the output of the rectifier circuit is low. This low output will cause a low cathode follower output, which again is consistent with the original assumption and will allow the circuit to remain in this state. The change from one state of the circuit to the other is made by means of the reset and read-in signals. When the reset signal becomes high level 1 will be high and assuming level 2 to have its normally high value, A' will become high. The reset signal should stay high during the time in which the output A' is changed from low to high so that A' will keep level 1 high after the reset signal returns to its normally low voltage. Once the circuit is in the state with A' high, it is no longer affected by the presence or absence of a reset signal. In order to change the voltage of A' from high to low the read-in

signal is made low. This will cause A' to become low, so that level 1 will be low and allow the circuit to remain in this state after the read-in voltage returns to its normally high value.

The circuit of Fig. 2-1 shows great similarity to a trigger pair and hence has been called a three-grid trigger pair. Figure 2-3

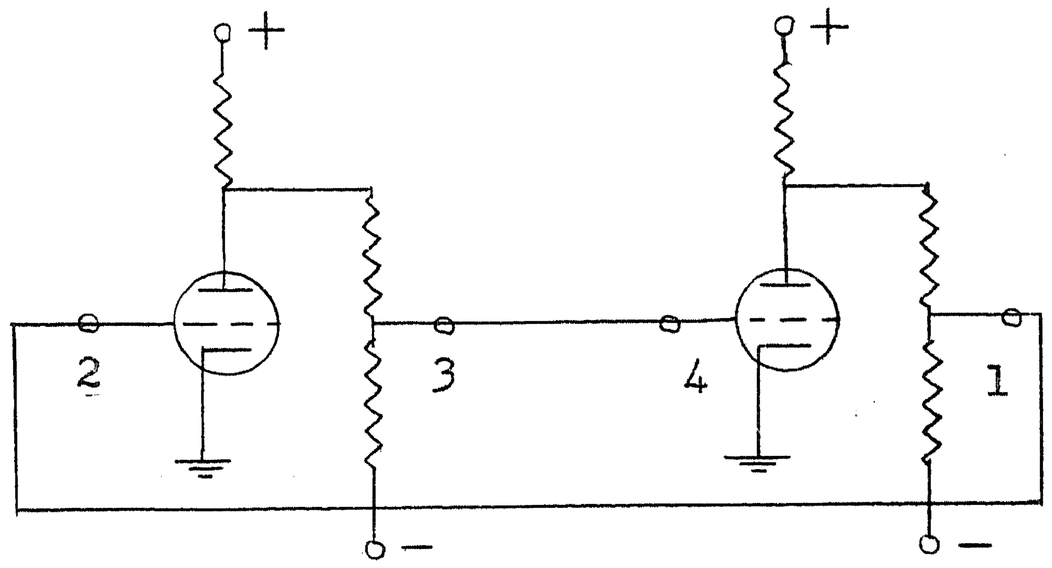


Fig. 2-3. Conventional Trigger Pair

shows the schematic diagram of a regular trigger pair. If in this diagram the connection 1 to 2 is replaced by a cathode follower and rectifier circuit the circuit of Fig. 2-1 is obtained. This operation can be repeated for the connection 3 to 4 to obtain the circuit of Fig. 2-4,

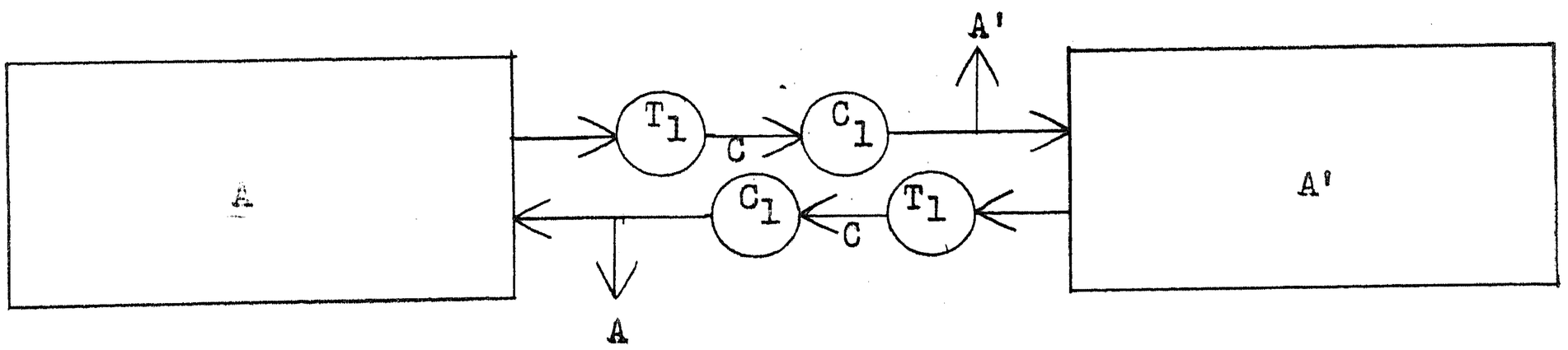


Fig. 2-4. Four-Grid Trigger Pair

which has been called a four-grid trigger pair. The conditions for the two rectifier circuits A and A' of this trigger pair are shown in Fig. 2-5.

	A	A'
1. hold	A	A'
2. read-in	read-in 0	read-in 1

Fig. 2-5. Conditions for a Four-Grid Trigger Pair

A low output of the cathode follower A will make the hold level of the circuit A low and as a result make the output A' high. This signal in turn controls the hold level of circuit A'. Hence the output of the rectifier circuit A' will be high provided that the read-in signal is in its normally high state. The high output of the rectifier circuit is consistent with the low output of the cathode follower A, so that the circuit will remain in the state with A low. This state has been called state 0. The state which has both the primed cathode follower output and the primed rectifier circuit output low has been called state 1. The operation of the trigger pair is symmetric with respect to the primed and unprimed outputs. The trigger pair is placed in state 0 when the input, read-in 0, becomes low. A low input, read-in 1, will place the trigger pair in state 1. Instead of using a normally high read-in signal on the read-in level, a normally low reset signal can be used on the hold level, as was the case for the three-grid trigger pair. This can be illustrated with the example of Fig. 4-31 which shows the conditions for the four-grid trigger pair FSTP 12. The hold level for FSTP 12' has as an input the normally low reset signal FSR. The other levels of this circuit are used for four modes of read-in, each of which will make the output FSTP 12' low. The output FSTP 12' can be made high

under control of the reset signal FSR or any of the three read-in conditions listed for the circuit FSTP 12. This example shows that read-in and reset signals from various origins can be combined in one trigger pair.

The facility with which various conditions can be used to control this kind of trigger pair proves a great advantage over the conventional trigger pair of Fig. 2-3. A second advantage is the saving in vacuum-tubes which the circuits of Figs. 2-1 and 2-4 represent. In order to make a comparison between the two types of trigger pairs, the circuits of Fig. 2-6 should be considered. These show a standard trigger pair,

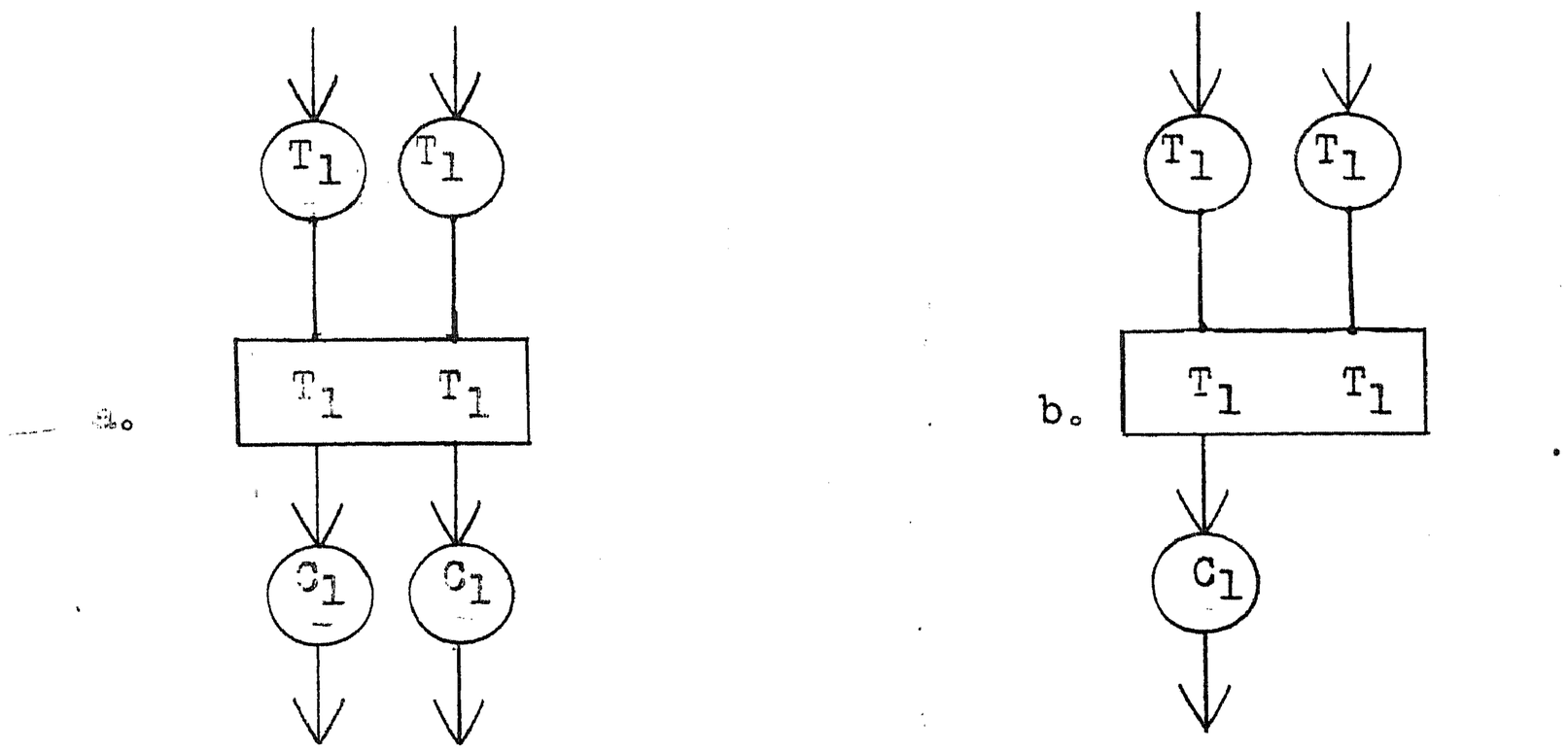


Fig. 2-6. Complete Conventional Trigger Pairs

complete with read-in puller tubes and output cathode followers. These circuits have the essential feature that the outputs can be used as inputs to other circuits of the same kind. The same characteristic is a property of the rectifier circuits shown in Fig. 1-15 and hence of the trigger pairs which use these rectifier circuits. The circuit of Fig. 2-6a which uses 6 vacuum-tube grids is equivalent to a rectifier trigger pair which requires 4 vacuum-tube grids only. A three-grid trigger pair is

equivalent to the circuit of Fig. 2-6b, using 5 grids. The limiting factor in the use of selenium rectifier trigger pairs is the speed at which the rectifier circuit can be operated.

Selenium rectifier trigger pairs which make use of positive sensing cards can be obtained in a manner similar to the one described above for negative sensing cards. Special adaptations to circuits using switches or relays can be made using the methods which were outlined at the end of the previous chapter. In the circuits described in Chapters 3 and 4 a total of 137 three-grid trigger pairs and 26 four-grid trigger pairs is used. All these trigger pairs use negative sensing cards.

Multiplets

The four-grid trigger pair of Fig. 2-4 can be considered as two separate circuits, A and A', with the outputs A' and A, respectively, which control each other. Each of these circuits is equivalent to the circuit shown in Fig. 1-15a. It has been mentioned in Chapter 1 that this circuit can be considered the basic unit of a design which employs rectifier circuits. The four-grid trigger pair illustrates that it is possible for two of these basic units to form a circuit with two stable states. The circuits which can be obtained by combining more than two of these basic units are called multiplets and will be discussed in this section.

A circuit using three basic units, called a triplet, is shown in Fig. 2-7. The conditions for the three rectifier circuits A', B' and C' are listed in Fig. 2-8. The read-in signals are normally high. When the signal, read-in 1, becomes low, the output of the rectifier circuit A' will be low and as a result the cathode follower output A will be high. This high output will make the hold levels of B' and C' high, causing the

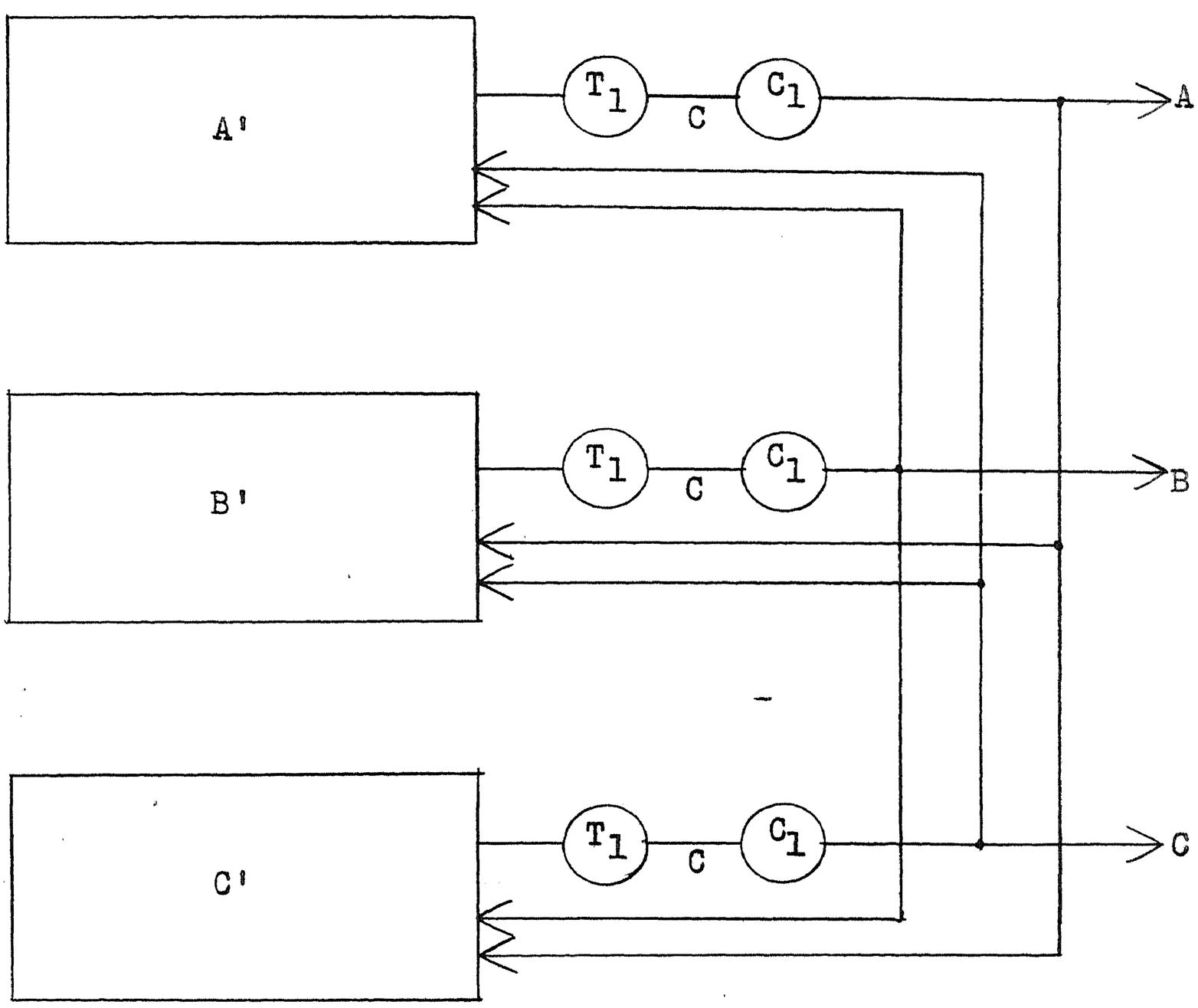


Fig. 2-7. Triplet

	A'	B'	C'
1. hold	B; C	C; A	A; B
2. read-in	read-in 1	read-in 2	read-in 3

Fig. 2-8. Conditions for a 3C2 Triplet

outputs B and C to become low. The hold level of A' which is controlled by B and C will now be low and will remain low after the read-in signal has returned to its normally high value. This shows that the triplet has a stable state with the output A high and the outputs B and C low. It follows from symmetry considerations that two other stable states can be obtained, in which B and C, respectively, are high. The three states of the triplet are listed in Fig. 2-9a. A high unprimed output is indicated

State	a. 3C2 triplet	b. 3C1 triplet
	A B C	A B C
1	1 0 0	0 1 1
2	0 1 0	1 0 1
3	0 0 1	1 1 0

Fig. 2-9. States of Triplets

by a 1, a low unprimed output by a 0. Figure 2-9b lists an alternate set of three states for a triplet. In this case two outputs are high and one is low. The conditions for a triplet of this kind (Fig. 2-10) show that two hold levels are necessary in addition to the read-in level. If it is desired to place the triplet in the state 1 both the signal, read-in B, and the signal, read-in C, should be made low. The method of changing

	A'	B'	C'
1. hold 1	B	C	A
2. hold 2	C	A	B
3. read-in	read-in A	read-in B	read-in C

Fig. 2-10. Conditions for a 3C1 Triplet

the state of a four-grid trigger pair by means of a normally low reset signal can also be applied to triplets. This is illustrated in Fig. 2-11

A'	hold	B; C; reset 2; reset 3
B'	hold	C; A; reset 3; reset 1
C'	hold	A; B; reset 1; reset 2

Fig. 2-11. Conditions for a 3C2 Triplet with Reset

which applies to the same triplet as does Fig. 2-8. In order to place the triplet in state 1 the hold levels of B' and C' should be made high. This is done in the given example by the input voltage, reset 1.

In order to describe the various types of multiplets more conveniently, the notation nCm will be introduced. The expression nCm represents the number of combinations, m at a time of n quantities. When used as the name of a multiplet it indicates the number of states which such a multiplet can assume. The letter n indicates the number of basic switching units of the circuit. Hence n is equal to the number of rectifier cards and 2n is equal to the number of vacuum-tube grids used. The letter m represents the number of outputs of the multiplet which are low at one time. With this notation the first triplet discussed in this

chapter (Fig. 2-8) can be described as a 3C2 multiplet and the second triplet (Fig. 2-10) as a 3C1 multiplet. In order to determine the state of a 3C1 triplet it is sufficient to sense for one low output or for two outputs which are high simultaneously. The state of the 3C2 triplet is determined by sensing for two simultaneous low outputs or for one high output. If it is desired to sense whether the triplet is in either of two states the conditions for these states should be combined. This may result in some cases in a condition of a simple nature. A low output A of the 3C2 triplet of Fig. 2-9a, for example, signifies that the triplet is either in state 2 or state 3. A practical application of a 3C2 triplet is the Slow Storage Triplet, which is described in Chapter 3 on page 3-17.

The number of states of an nCm multiplet is given by the table of binomial coefficients. These numbers are listed in Fig. 2-12 together with the number of hold levels necessary for each of the n rectifier circuits. Negative sensing cards are assumed in each case. With m outputs low for each state of the multiplet, one of the outputs will be high for the combinations, m at a time, of the remaining n-1 outputs. Each of these combinations requires a separate hold level for the rectifier circuit which controls the high output. Thus the expression (n-1)Cm indicates the number of hold levels for the rectifier circuits of the multiplet. With (m+1) rectifiers for each hold level and a total of n cards, the number of rectifiers which is necessary for an nCm multiplet becomes $n \cdot (m+1) \cdot \left[(n-1)Cm\right]$. This quantity is also listed in Fig. 2-12. The rectifiers for the read-in or reset signals are not included in these numbers. It can be seen from Fig. 2-12 that the number of rectifiers required for the larger types of multiplets tends to become prohibitive. The trivial cases of nC0 or nCn multiplets, which have one state only, are not listed.

Type	Number of States	Number of Hold Levels per Card	Total Number of Rectifiers
2C1	2	1	4
3C1	3	2	12
3C2	3	1	9
4C1	4	3	24
4C2	6	3	36
4C3	4	1	16
5C1	5	4	40
5C2	10	6	90
5C3	10	4	80
5C4	5	1	25
6C1	6	5	60
6C2	15	10	180
6C3	20	10	240
6C4	15	5	150
6C5	6	1	36

Fig. 2-12. Number of States, Levels and Rectifiers of Multiplets

The number of states of a multiplet can be reduced by omitting the hold levels of the states which are not desired. As an example the conditions for the hold levels of a 5C2 multiplet are shown in Fig. 2-13. The outputs of the multiplet are numbered 1, 2, 3, 4 and 5. The ten states which this multiplet can assume are numbered according to the list of Fig. 2-14. These numbers are used in Fig. 2-13 to indicate the state to which each hold level belongs. Figure 2-13a shows the hold levels for the complete multiplet. A multiplet of this type has been used in

Card	State	Hold Levels		
		a. complete	b. omit 9	c. omit 1,3,8,9
5'	3	2 1	2 1	
	4	4 2	4 2	4
	5	4 3	4 3	
	6	4 1	4 1	
	8	3 1	3 1	
	9	3 2		
4'	7	5 1	5 1	5
	8	3 1	3 1	
	9	3 2		
	0	5 3	5 3	
	2	5 2	5 2	
	3	2 1	2 1	
3'	1	5 4	5 4	
	2	5 2		2
	3	2 1	2	
	4	4 2		
	6	4 1	4 1	1
	7	5 1	5 1	
2'	5	4 3		
	6	4 1	4 1	
	7	5 1	5 1	1
	8	3 1	3	3
	0	5 3		
	1	5 4	5 4	
1'	9	3 2		
	0	5 3	5 3	
	1	5 4	5 4	
	2	5 2	5 2	2
	4	4 2	4 2	
	5	4 3	4 3	3

Fig. 2-13. Conditions for Complete and Incomplete 5C2 Multiplets

Mark IV Slow Storage (see Chapter 3, page 3-8). The conditions for a multiplet which can assume the states 0 - 8 only are shown in Fig. 2-13b. It would be sufficient to remove one of the hold levels for state 9 to obtain such a multiplet. This procedure may be of use in the case of a reset operation. In Fig. 2-13b, however, all the conditions which are

State	5 4 3 2 1
0	0 1 0 1 1
1	0 0 1 1 1
2	0 1 1 0 1
3	1 1 1 0 0
4	1 0 1 0 1
5	1 0 0 1 1
6	1 0 1 1 0
7	0 1 1 1 0
8	1 1 0 1 0
9	1 1 0 0 1

Fig. 2-14. States of a 5C2 Multiplet

necessary for state 9 have been omitted. The process of reducing the number of stable states for a multiplet can be continued as is shown in Fig. 2-13c, which shows the conditions for a 5C2 multiplet with six stable states. It is apparent from these conditions that the 5C2 multiplet has "degenerated" into the trigger pair 4-5 and the triplet 1-2-3.

The remarks which have been made concerning the read-in and the read-out of triplets can be extended to the general case of an nCm multiplet.

The application of multiplets is limited by the number of rectifiers which they require. In many cases it is more desirable to use a number of three- or four-grid trigger pairs instead of a large multiplet.

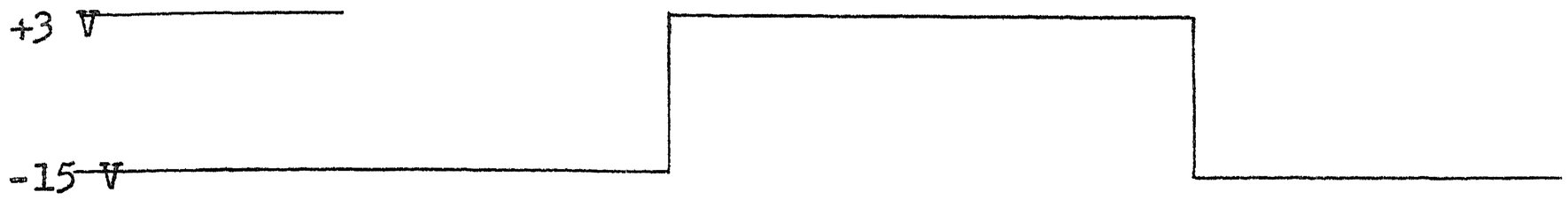
Multivibrators

The method which has been used to obtain a four-grid trigger pair from the standard trigger pair of Fig. 2-2 can be applied also to the one-shot multivibrator circuit of Fig. 2-15a or to the regular multivibrator circuit of Fig. 2-15b. In this way the selenium rectifier multivibrator circuits of Fig. 2-16 are obtained. The resistor and

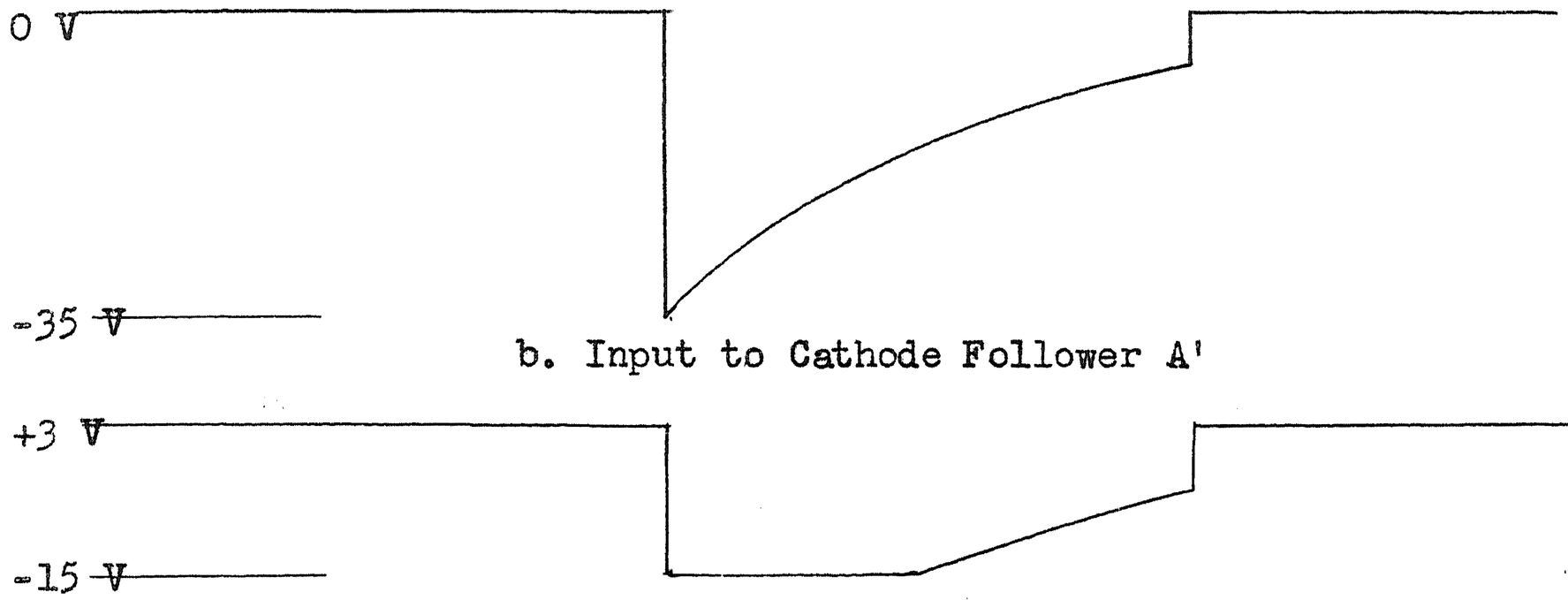
Fig. 2-15. Conventional Multivibrators

Fig. 2-16. Selenium rectifier Multivibrators

condensor network is indicated in each of the schematic diagrams. The circuit of Fig. 2-16a has a normal state with the output A' high. This state will be changed when the circuit A' is made low or the circuit A is made high. The circuit remains in this new state until the condensor C has been charged, after which the circuit returns to its normal state. Figure 2-17 shows the waveforms for the cathode follower output signals A and A' and for the input to the cathode follower A'. The regular cycle can be abrogated under control of a read-in signal to A or a reset signal to A'. The circuit can be reduced to a three-grid circuit either by omitting the output A' with the corresponding rectifier circuit or by omitting the circuits marked A.



a. Output of Cathode Follower A



b. Input to Cathode Follower A'

c. Output of Cathode Follower A'

Fig. 2-17. Multivibrator Waveforms

Figure 2-16b shows the selenium rectifier circuit which is equivalent to the regular multivibrator circuit of Fig. 2-15b. The circuit can be engaged in one of two modes of operation. With the outputs of the rectifier cards of A and A' both high, the circuit will remain in a state which has the outputs A and A' high. This state can be changed by means of a read-in to A. During the time that the read-in signal is low the outputs will remain high, but condensor C will be discharged. When the read-in signal becomes high again the output A' is made low and condensor C' is discharged. The state of the multivibrator changes when the condensor C becomes charged. The circuit continues this mode of operation until one of the rectifier circuits is kept high during one cycle. The cycling of the multivibrator will be suspended when one of the rectifier circuits is kept low. The cycling is resumed when the low signal is removed. The circuit of Fig. 2-16b can be reduced to a three-grid circuit in the same way as described for the one-shot multivibrator.

B. Cycling of Multiple State Circuits

Conditions for Cycling

In Part A of this chapter the read-in to multiplets by means of normally high read-in signals or by means of normally low reset signals has been discussed. It has been assumed in this discussion that the read-in is independent of the state of the multiplet prior to the read-in. It will be shown in the following paragraphs that it is possible to introduce conditions which allow the read-in to occur only for a selected number of states of the multiplet. Such a read-in is called a restricted read-in. A series of successive restricted read-ins is called a cycle.

The terms "restricted read-in" and "cycle" can apply also to a group of multiplets. In this case the read-in to one of the multiplets is dependent upon the state of this multiplet and upon the states of the other multiplets. A group of multiplets which has this kind of mutually dependent read-ins is called a ring.

It will be assumed throughout this and the following chapters that the conditions which control a restricted read-in will remain unchanged during the entire read-in operation. The immediate consequences of this assumption are twofold: a) The state of the multiplets prior to the read-in and the state after the read-in have in common the output voltages which are used to control the change-over. b) Once the desired state of the multiplets has been obtained, no further changes may be affected under control of the read-in signal. It follows immediately from b) that at least two distinct read-in signals are required to step a ring through a cycle. It follows furthermore that the cycling of the ring is independent of the duration of the read-in signals. With the

cycling also independent of the time interval between read-in signals, the discussion of a series of read-in operations can be restricted to the order in which the states of the ring are assumed, without reference to the time intervals which are involved. The change from one state of a multiplet or ring to the next is called a step. The read-in or reset signals which cause a step are often called pulses.

Cycling of Multiplets

The restricted read-in and the cycling of an nCm multiplet will be discussed first for those cases where a normally high read-in signal is used. A read-in to the multiplet can be restricted by the requirement that a given set of p outputs of the multiplet be low. These p outputs will be low in (n-p)C(m-p) states of the multiplet. The state to which the multiplet is to be stepped is one of these states. Thus the number of s steps which can be taken under control of a restricted read-in is given by:

$$s = (n-p)C(m-p) - 1.$$

In order that the multiplet may be stepped through all its states in a prescribed order, the quantity s should equal 1. This requires that (n-p)C(m-p) equals 2, which is the case only for (n-p) = 2 and (m-p) = 1 or p = (m-1) = (n-2). The smallest multiplet for which this is possible is the triplet 3C2. In general the multiplet will be of the type nC(n-1). A multiplet of this type has n stable states. It should be noted that any two states have (n-2) low outputs in common. Hence the multiplet can be made to step through the n states in any specified order. In total (n-1)! different cycles are possible. At least two pulses are necessary

for a cycle, when n is even. A minimum of three pulses is required when n is odd. Figure 2-18 shows the conditions which are necessary to cycle a 3C2

	A'	B'	C'
1. hold	B; C	C; A	A; B
2. read-in	B; γ	C; α	A; β

Fig. 2-18. Triplet with Cycling Control

triplet under control of the pulses α, β and γ. The order of the states is 1, 2, 3 as defined in Fig. 2-9a. The Slow Storage Triplet (page 3-17) has a cycle in which two steps are made with a restricted read-in. The read-in to the home position of the triplet is unrestricted.

An alternate method for the restricted read-in of a multiplet is the use of a normally low reset signal in the hold levels of the multiplet. This method can be used without any restrictions with multiplets of the type nCl. As an example the conditions for a 4Cl multiplet which steps through its four states under control of the reset pulses α and β is shown in Fig. 2-19. The outputs are low in the order A, B, C, D.

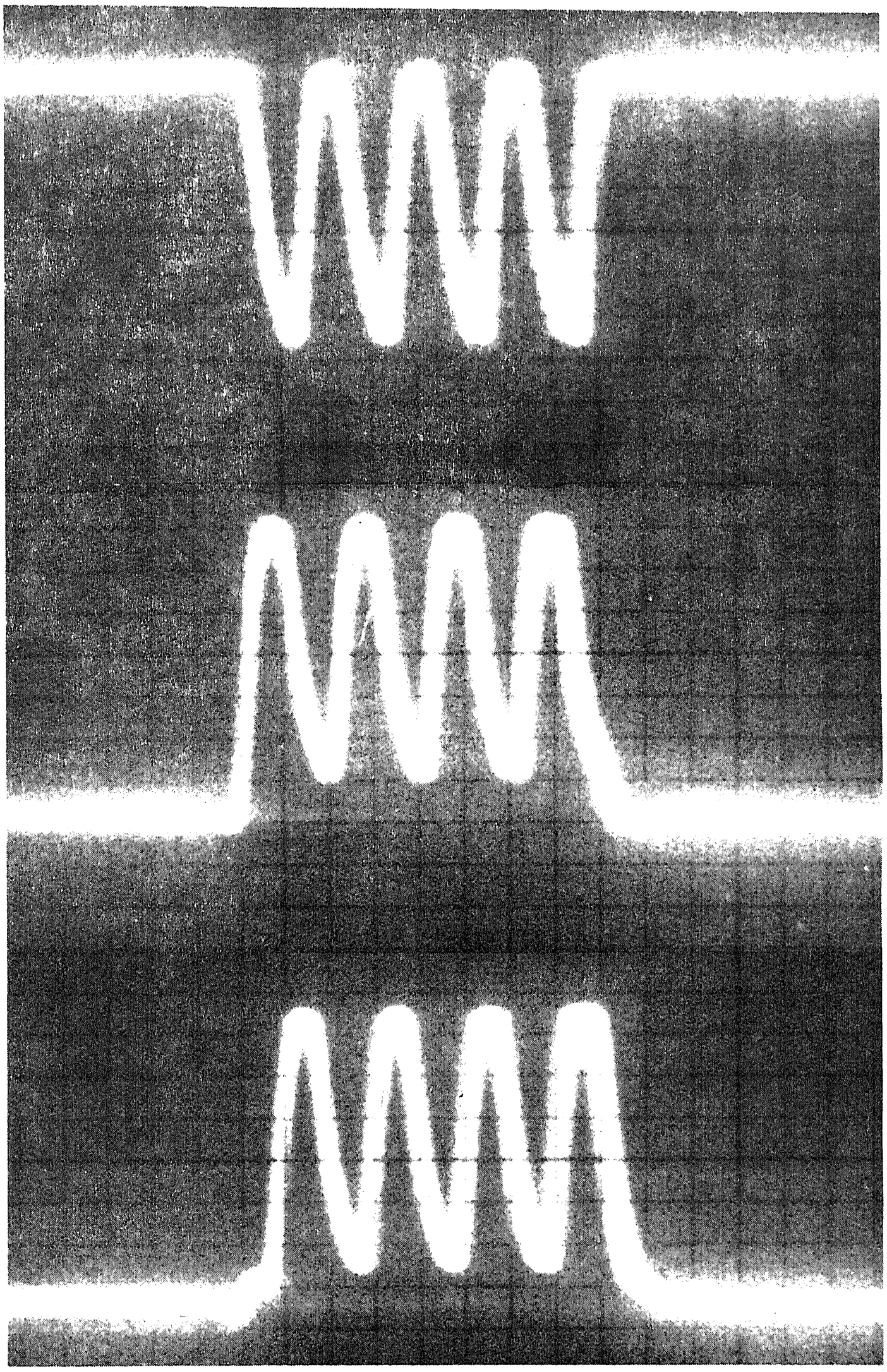
	A'	B'	C'	D'
1. hold	B	C	D	A
2. hold	C	D	A	B
3. hold	D; β	A; α	B; β	C; α

Fig. 2-19. 4Cl Multiplet with Cycling Control

In some applications it may desirable to perform two steps in rapid succession. In such a case the control pulse input of the second step can be omitted, causing the second step to take place immediately after the first step is performed. This procedure can be extended to more steps by omitting inputs of the corresponding controlling pulses. When all pulses are omitted the multiplet will be "free cycling," that is, it will step continuously. The time which is required for a complete cycle is a function of the time delay of the rectifier cards. Figure 2-20 shows the output signals of a free cycling triplet. The conditions for this triplet are those of Fig. 2-18, with the signals β and γ at a constant low voltage. The signal α is low during 22 microseconds. The triplet completes four cycles during the time in which α is low. This indicates that about 6 microseconds are necessary for one cycle. The minimum time during which a read-in signal should be low in order that the multiplet will change to the desired state is called the response time of the multiplet. The response time for each of the three steps of the free cycling triplet is 2 microseconds. It can be seen from Fig. 2-20 that the triplet reaches a stable state before the cathode follower output returns to -15 V. Hence the response time of the triplet is shorter than the decay time of the rectifier circuits. The rectifier circuits used for the triplet were of the type E20 (Fig. 4-87). The frequency of the free cycling triplet changes rapidly for small voltage fluctuations. A response time of 2 microseconds has been observed also for the three- and four-grid trigger pairs used in the circuits of Chapters 3 and 4.

Cycling of Rings

It has been found in the previous section that a multiplet of the type nC(n-1) can be stepped through all possible states in any desired



Oscillographs of a Free Cycling Triplet

Fig. 2-20.

order. When more than one multiplet of this type is used in a ring the number of stable states of the ring is the product of the possible states of each component multiplet. If the number of low outputs for the ring is again called p, then there will be only two states of the ring in which (p-1) specified outputs are low. Hence it is possible to use these (p-1) outputs to control one step of the ring. It is, however, no longer possible to perform a step between any two states of the ring. Only those states which differ in two outputs only can be used as successive states in a cycle.

It is possible to consider a ring as one large multiplet, from which a sufficient number of states is removed to make each restricted read-in apply to two states only. Thus by removing four states from a 5C3 multiplet a circuit can be obtained which is equivalent to a trigger pair and a 3C2 triplet, and which can cycle through all six remaining states.

The simplest building block of a ring is a 2C1 multiplet, or four-grid trigger pair. It can be verified from the formula for s on page 2-18 that a single trigger pair cannot step between its two states. With n trigger pairs 2^n states can be obtained. The ring can cycle through these 2^n states provided that the state of only one trigger pair is changed during one step.

Four rings using four-grid trigger pairs have been used in the circuits of Chapters 3 and 4. One of these, the Slow Storage Control Ring, is in part controlled by a triplet.

Superposition of Switching Operations

The fact that a basic switching unit can combine several "and" conditions by one "or" condition makes it possible to perform with one

circuit more than one operation. Each of these operations may require several "and" conditions. The operations can in general be distinguished in two ways: a) The operations are performed at different moments. Hence the output of the switching unit should be sensed at the proper moment for each of the operations which are performed. b) The operations are performed only when a control signal is present. The control signals for the different operations should not overlap.

The method of superposing operations can be applied to all circuits which make use of the basic switching unit. In particular, in the trigger pair and ring circuits a considerable saving in equipment can be achieved in this way. The circuit JCTR is an example of a trigger pair which performs two operations, each at a different moment. The functions of this trigger pair are described on pages 4-25 and 4-28. When applied to rings the method of superposition will make it possible to perform any number of cycles with the same circuits. This is well illustrated by the Main Control Ring of the Sequence Unit (Chapter 4, Part J). A further application of the superposition principle is shown in the circuits FSTP 7-10 and FSTP 11-14 (Chapter 4, page 4-27). Each of these groups of four trigger pairs forms a ring. The ring may be placed in any of six initial states. Under control of four successive pulses each of these states will be changed to a final state. The six final states are distinct. The ring will step through a different cycle for each of the six cases. However, several states of the ring occur in more than one cycle at different moments. This example illustrates the way in which a ring can be used to perform a translation from an initial state to a final state.

CHAPTER 3

SLOW STORAGE UNIT OF MARK IV

A. Organization of the Mark IV Calculator

The Mark IV Calculator consists of four main parts: a) the Storage System; b) the Arithmetic Units; c) the Input-Output System; and d) the Sequence Unit. The interrelation of these parts is shown in the simplified block diagram of Fig. 3-1. The interconnecting bus system of the calculator is indicated in this diagram by single lines. One number may be transferred at a time in the direction of the arrows. The machine is divided in two sides, the β side and the γ side, which are connected by two busses, the Fast Out-Bus and the Fast In-Bus. The units on the β side read out onto the Fast Out-Bus and read in from the Fast In-Bus. The units on the γ side read out onto the Fast In-Bus and read in from the Fast Out-Bus. Numbers remain stored in the units from which they are read out until they are destroyed upon read-in of a new number. Numbers can be read only from a β unit to a γ unit or vice versa.

Storage System

The storage system of the calculator can be divided in three parts: a) Fast Storage; b) Slow Storage; and c) Special Registers.

The Fast Storage consists of 210 registers, each able to store a 16 digit number and its algebraic sign. Digits are represented by a coded decimal number system using four binary digits. Numbers are read out of the registers in series. The time necessary to read one number is the basic cycle of the calculator. This is called a number time. The time necessary to read one digit is called a digit time. In a number time there are twenty digit times, numbered 0 digit time (DT) to 19

digit time. A number time begins with 18 DT, followed by 19 DT, 0 DT, 1 DT and so on up to 17 DT. All Fast Storage registers are β units.

The Slow Storage unit can store 4000 numbers on the surface of a magnetic drum. The drum storage has a slow access time, which is in part compensated by storing or reading groups of ten numbers at a time. The drum storage belongs to the β side of the machine. It is connected to the bus system through 20 transfer registers. These transfer registers can be used in the same way as the Fast Storage registers.

The Special Registers include the following:

a) γ Transfer Register, also used as External Transfer Register.

b) β Transfer Register, also used as Shift and Normalize Register.

c) Shift Control Register.

d) Call Register.

e) Line Number Register.

f) I-J Register.

g) K Register.

h) Condition Register.

i) Slow Storage Control Register.

These registers, with the exception of the γ Transfer Register, belong to the β side of the machine. Their special functions will not be discussed in detail.

Arithmetic Units

The following Arithmetic Units are available: a) Two Accumulators; b) Multiply Unit; c) Divide Unit. All Arithmetic Units are located on the γ side of the machine.

Each Accumulator is able to add a number to a previous sum during one number time. The read-in to an Accumulator can be with reset or

accumulative. Special provisions are available to add numbers of n x 16 digits.

The Multiply Unit is able to multiply two numbers during 8 number times following the read-in of the multiplicand and the multiplier. The calculator can be used for other operations during the 8 number times of the multiply cycle.

The Divide Unit is able to divide one number by another number during 20 number times following the read-in of the dividend and the divisor.

Input-Output System

The input to the calculator and the output produced by the calculator are recorded on magnetic tapes. Tapes can be recorded: a) by the Record Unit of the calculator; b) by the Tape Preparation Table; c) by the Coding Machine. Numbers are recorded in the same fashion by all three units. The numbers prepared by the Coding Machine are used by the Sequence Unit to control the calculator. Tapes can be read: a) by the Read Unit of the calculator; b) by the four Printers.

The Tape Preparation Table, the Coding Machine and the Printers are auxiliary units which operate independently of the calculator. They are used to prepare problems for the calculator and to print out the results computed by the calculator. The Tape Preparation Table and the Coding Machine are manually operated. The Printers employ electric typewriters. An average of 20 number times is required to read one number from tape or to record one number on tape. Eleven tape mechanisms are available, each of which can be connected to the Record Unit, to the Read Unit or to a Printer.

Sequence Unit

The Sequence Unit is used to control the operations of the calculator through a series of codes. Each code controls the calculator during one number time. A storage capacity for 10,000 codes is available on the magnetic drum. Each storage location is identified by a number, called the line number. Codes are generally read in series with increasing line numbers, but it is possible to interrupt such a series of codes and start a new series beginning with another line number. This is referred to as a call operation. A code consists of three independent parts: the α code, the β code and the γ code. The β code identifies a β unit; the γ code identifies a γ unit; the α code dictates the direction of transfer and the sign with which the transfer is to take place. The Sequence Unit also has provisions for manual control of the calculator.

A detailed description of the Slow Storage Unit will be given in the following parts of this chapter. The Sequence Unit will be discussed in Chapter 4.

B. Operation of the Slow Storage Unit

The 210 Fast Storage registers of Mark IV consist of magnetic delay lines. The time required to read out a number, together with additional time for switching operations, is 1.2 milliseconds, or one number time. In addition to the 210 delay lines, a magnetic drum is used for a Slow Storage of 4000 numbers. The access time to the numbers on the drum is longer than the access time to the numbers in the delay lines since the Slow Storage pole pieces are selected by relays, and since a varying time delay is introduced in waiting for the right number location to appear under the selected pole piece. Numbers are transferred in groups of 10 either from the drum to the transfer registers or from the transfer registers to the drum. This transfer takes place while the machine continues to compute from Fast Storage.

The magnetic drum rotates with a speed of 2000 r.p.m., and thus requires 30 milliseconds for one revolution. This time is equal to 25 number times and suggests that 25 numbers be stored in a single channel around the drum. With a drum diameter of 22 inches each number would take up 2.76 inches of the circumference. Since a number is stored using 20 pulses the pulse density would be 7.25 pulses per inch, and the pulses would be read with a frequency of 15 kilocycles. It is, however, possible to increase both the pulse density and the frequency by a factor of four. Thus, in order to use the drum surface with the desired efficiency the pulses of four sets of 25 numbers are interlaced on one channel. In this way 100 numbers are stored per channel. For a total capacity of 4000 numbers, 40 decimal channels are required.

The codes used to control the Slow Storage Unit are the following β codes:

Code	Function
0200	Register S_0
--	---
0209	Register S_9
0210	Register S_0'
0219	Register S_9'
1201	Slow Storage Control Register in and S in from the drum
1211	Slow Storage Control Register in and S out to the drum
1221	Slow Storage Control Register in and S' in from the drum
1231	Slow Storage Control Register in and S' out to the drum
3200	Slow Storage Control Register.

From this list it can be seen that ten delay line registers, the group S or S', are used at a time to transfer numbers to or from the magnetic drum. The other ten registers are at that time available as Fast Storage Registers. In addition there is a Slow Storage Control Register, which stores a control number in the range 0000-3999. This number specifies the location on the drum where the first number in the group of ten is to be read or recorded. The other nine numbers follow in order. The hundred's and thousand's digits of the control number select one of the 40 decimal channels, 00-39. The position around the circumference of the drum is determined by the unit's and ten's digits of the control number. The four interlaced groups of 25 numbers in each channel are numbered 0-24, 25-49, 50-74 and 75-99, corresponding to the unit's and ten's digits of the control number. Each of these groups of numbers has its own set of record pulses for recording on the drum and a corresponding set of advance pulses for reading back from the

drum. The selection of the channel and of the set of pulses to be used is complicated by the possibility of switching from one channel to the next or from one set of pulses to the next during the time in which the 10 numbers are transferred.

When a slow-fast or fast-slow transfer is in progress no codes may occur which would interfere with this operation. To ensure this a Wait circuit is used in the Sequence Unit, as described in Chapter 4, page 4-44. A wait will be introduced in the following situations:

1) When the group of registers S_0 - S_9 is engaged in a transfer and a read-in or read-out code for these registers occurs.

2) When the group of registers S_0' - S_9' is engaged in a transfer and a read-in or read-out code for these registers occurs.

3) When a code to read in to the Slow Storage Control Register occurs while a transfer operation is in progress. A transfer operation does not prevent a read-out from the control register.

A block diagram of the Slow Storage Unit, Fig. 3-2, shows that numbers may be read from the transfer registers through the record unit and the channel selection relays onto the drum. The number flow in the opposite direction is from the drum through the relays and the playback unit to one of the two groups of transfer registers. The transfer registers S and S' are connected to Fast Storage through the Fast In-Bus and the Fast Out-Bus. The read-in and read-out operations to that part of the machine are controlled by sequence codes. The read-in and read-out to the storage drum are controlled by the Slow Storage timing circuits. The Slow Storage Control Register is shown in the lower part of the diagram. Numbers are read into the Slow Storage Control Register from the Fast In-Bus and may be read out onto the Fast Out-Bus. The method used in describing the rectifier switching operations of Slow Storage conforms to the method used for the circuits of the Sequence Unit, as explained in Chapter 4, Part B.

C. Slow Storage Control Register

The indicated schematic diagram of the Slow Storage Control Register and of the associated read-in and read-out circuits is shown in Fig. 3-3. The part of the register which stores the unit's and ten's digits of the control number consists of three-grid trigger pairs using selenium rectifier circuits. The digits are stored in a 5C2 number system. The hundred's digit of the control number is stored in a multiplet using the same number system. The thousand's digit, which may assume the values 0, 1, 2 or 3, is stored in the two four-grid trigger pairs SCRTH2 and SCRTH1. The read-in to the register is controlled by the circuits SCRRI' and SCRR. The conditions for these circuits are shown in Fig. 3-4. The output SCRRI' will be low during one number time for any of the five codes which control a read-in to the register. The circuit senses for the β code only and will be low regardless of the α code. SCRRI', together with the signals 0 DT' and β-out, controls the reset signal, SCRR, which will be high only in the case of a read-in.

The conditions for one of the unit's and one of the ten's trigger pairs are shown in Fig. 3-5. The read-in operation is performed through level 2 of these circuits. The unit's digit is read in during 2 digit time from the Fast In-Bus, the ten's digit is read in from this bus at 3 digit time. Level 1 is in each case the hold level. The trigger pairs are reset through the signal SCRR, which becomes high during 0 digit time, preceding the read-in. Figure 3-5 also shows the conditions for one of the circuits of the hundred's multiplet. The reset signal is not used in the multiplet circuit.

The conditions for the two thousand's trigger pairs are shown in Fig. 3-6. These conditions are more complicated since the control

register has been made cyclic. The numbers 0000 - 3999 are read in from the bus without a change. If a number larger than 3999 appears on the bus, the number read into the register will be smaller than this number by a multiple of 4000. The sign of the number is disregarded in each case. Because of this cyclic read-in to the control register, the state of the thousand's trigger pairs is determined by the thousand's and the ten thousand's digits appearing on the bus. Table 3-1 shows the digits on the Fast In-Bus

Table 3-1

Thousand's Digit Read into Slow Storage Control Register

Digit on Bus		Digit in SCR		
			Binary	
Ten Thousand's	Thousand's	Decimal	SCRTH-2	SCRTH-1
even (0,2,4,6,8)	0	0	1	1
	1	1	1	0
	2	2	0	1
	3	3	0	0
	4	0	1	1
	5	1	1	0
	6	2	0	1
	7	3	0	0
	8	0	1	1
	9	1	1	0
odd (1,3,5,7,9)	0	2	0	1
	1	3	0	0
	2	0	1	1
	3	1	1	0
	4	2	0	1
	5	3	0	0
	6	0	1	1
	7	1	1	0
	8	2	0	1
	9	3	0	0

and the corresponding digits stored in the thousand's trigger pairs. The outputs of the trigger pairs SCRTH2' and SCRTH1' are represented by the binary digits 0 and 1. A one indicates that the primed output of the

trigger pair is low, and the unprimed output high. The inverse state of the trigger pair is indicated by a zero.

The read-in to the thousand's trigger pairs takes place in two steps. During 5 digit time the thousand's digit is read in. This read-in is performed with a translation, causing the output SCRTH2' to become low for a 0, 1, 4, 5, 8 or 9 and the output SCRTH1' to become low for all even digits. If the ten thousand's digit of the number which is read in is even, no further change is introduced. Table 3-1 shows that for an odd ten thousand's digit the trigger pair SCRTH2 should be changed to its inverse state. This is accomplished by making use of the trigger pair SCRTHO' (Fig. 3-7). This trigger pair has a read-in during 5 digit time and stores the same information as the trigger pair SCRTH2. This information is used during 6 digit time and causes SCRTH2 to change to its inverse state. The two trigger pairs SCRTH2 and SCRTHO together form a four-state ring. The states of this ring, together with the circumstances under which they occur are shown in Table 3-2.

Table 3-2

Digit time	SCRTH-2	SCRTH-O	
5 DT	1	0	read in 0 or 1
6 DT	0	0	change to 2 or 3
5 DT	0	1	read in 2 or 3
6 DT	1	1	change to 0 or 1

The read-out from the Slow Storage Control Register to the Fast Out-Bus is performed by the circuits SCR08-1 (Fig. 3-8). This operation is similar to the read-out from the I, J and K Registers as described in Chapter 4, page 4-32.

D. Relay Selection

Each of the 40 decimal channels in the Slow Storage section of the magnetic drum may be connected through a relay to the playback and record circuits. A decimal channel consists of four tracks, which store in parallel the binary components of the decimal digits. The channel selection relays (Fig. 3-9) are equipped with four normally open contacts, each of which can connect one pole piece to a playback and record unit. The selection of the relays is performed in two stages. First the information from the control register and the timing circuits is combined in the circuits HR and THR. These are standard selenium rectifier switching circuits, the outputs of which are inverted and fed to cathode followers. The voltage swing of the cathode follower outputs is of the order of 30 V. These signals are used to control the relay puller tubes. The low cut-off voltage of these tubes necessitates the large voltage swing. As a result the selection matrix for the puller tubes has been built with a larger size rectifier, consisting of four rectifier plates stacked together, thus allowing a larger back voltage. The large capacitance of this type selenium rectifier is admissable in this application, because the speed of the circuit is governed by the response time of the relays. The rectifier matrix is controlled by the nine signals HR and THR. The 40 output wires sense for one high signal of THR and two high signals of HR.

An example of the conditions for HR and THR is shown in Fig. 3-10. The circuits operate for two different situations.

1) The control number has any of the values --00 up to and including --90. In this case all ten numbers read from or to the drum are located in the same decimal channel. Only one relay will be picked up during the transfer operation. The output ST3 is low in this case, and as a result the outputs

HR correspond directly to the outputs of SCRH. One of the four outputs THR will be high.

2) The control number has any of the values --91 up to and including --99. The first numbers transferred to or from the drum will be located in the channel which corresponds to the hundred's and thousand's digits of the control number. The rest of the ten numbers transferred will be located in the next decimal channel. In this case the transfer is performed in the following fashion:

a) The relays are picked up as under 1, with the output ST3 low.

b) The transfer of the numbers in the first channel is performed.

c) The transfer is stopped after the number in location --99 has been read or recorded and a wait of one entire drum revolution is introduced.

d) During this revolution the signal ST3 becomes high and the signal ST1 becomes low. The relay for the second channel is picked up under control of levels 2-5 on the HR circuits, and level 2 on the THR circuits.

e) The transfer is resumed beginning with the number location --00. After the transfer is finished ST3 becomes low again and ST1 high.

The control for the outputs ST3 and ST1 is discussed in Part E. With ST1 low, the inputs to HR are translated in such a way that the "add 1" operation is performed. The "add 1" operation for THR is conditioned by the requirement that the hundred's multiplet stores a 9. It should be noted that as the output of THR becomes high level 1 of THR1 is made high through the first level return voltage, thus preventing THR1 and THR2 from being high at the same time.

The use of a multiplet to store the hundred's digit of the control number involves rectifier circuits which are more complicated than the circuits required by five three-grid trigger pairs. The increase in the

number of rectifiers is compensated by a reduction in the number of vacuum tubes used. The advantage of the multiplet is the fact that only two of its outputs can be low simultaneously. As a result only two of the outputs HR will be high at one time. The circuits for THR ensure that only one of these outputs will be high, so that only one of the 40 channel selection relays is pulled.

The type of relay which is used for the channel selection is expected to operate in 10 milliseconds, or 8 machine cycles. The time alloted for relay switching is at least 15 cycles, or 18 milliseconds. This delay can be reduced to any smaller number of cycles without adding any circuit elements. The timing is controlled by the Slow Storage Control Ring.

E. Timing Circuits

The operations of the Slow Storage Unit are initiated by any of the codes β1201, β1211, β1221 or β1231 as listed in Part B. These codes are present for one number time only. During the following cycles the Slow Storage Unit operates independently of the sequence commands under control of the timing circuits shown in Fig. 3-11. The main components of the timing circuits are: a) the Slow Storage Control Ring, SR, which provides the timing of the transfer operations; b) the Slow Storage Triplet, ST, which operates when it is necessary to switch from one channel to the next channel; and c) the trigger pairs, SS200, SS210 and SSRR, which indicate the type of transfer which is desired. The operation of each of these units will be discussed in turn.

The Slow Storage Control Ring consists of four sets of four-grid trigger pairs using selenium switching circuits. Its function is threefold: a) it provides the time delay necessary to allow the relays to pick up; b) it determines, with the aid of matching circuits, the time during which the numbers should be transferred; and c) it provides the signals used in the delay line advancing circuits. The control ring steps through the cycle of ten steps shown in Table 3-3. The four trigger pairs of the ring are identified by the names SR4, SR3, SR2 and SR1. A low signal at the primed output of the trigger pairs is indicated by a 1, a high output is indicated by a 0. Table 3-3 also shows the conditions which are required for a change from one state to the next. The ring is automatically reset to its home position when the machine is stopped. This is done by means of the -45 V signal obtained from the relay N1. The negative voltage will be removed when the machine is stopped. This is discussed in Chapter 4, page 4-54. The conditions for the selenium rectifier circuits of the control

Table 3-3

	SR	4	3	2	1	
1)		0	0	0	0	SCRRI'; OOXX; βUll'; ODT' → 1'
2)		0	0	0	1	OOXl; m'; 4DT' → 2'
3)		0	0	1	1	XXll; m'; 2DT' → 3'
4)		0	1	1	1	OlXX; M-5'; ODT' → 2
5)		0	1	0	1	OlOX, m+4'; lODT' → 1
6)		0	1	0	0	XlXO; ST2; ST3; l8DT' → 4'
7)		1	1	0	0	llXX; m+4'; lODT' → 2'
8)		1	1	1	0	XXlO; l8DT' → 3
9)		1	0	1	0	lOXX; m+4'; lODT' → 2
10)		1	0	0	0	XOOX; l8DT' → 4

ring are shown in Fig. 3-12. The ring leaves its home position under control of the signal SCRRI' and the signal βU11'. The steps which follow are made under control of the signals m', m+4' and M-5'. These signals are used to locate the position of the numbers to be transferred. This is done with the aid of the signals obtained from the number ring and the phase ring used in the Sequence Unit (Fig. 4-78). The number ring has five outputs, labelled 0 NT',..., 4 NT', which are low during successive number times. The phase ring has the outputs 0 P',..., 4 P', which are low during one phase. A phase is a time interval of five number times, beginning with 0 NT'. A combination of one phase and one number time identifies one of twenty-five number times and is used to identify a number location on the circumference of the drum. The outputs of the control register are combined with the number time and phase signals in such a way that the output m' is low during the number time of the desired number location. By permuting the number time inputs, the output m+1' is obtained which is low one number time after m'. The same method of permutation is used to obtain the outputs m+2', m+3' and m+4'. The output M-5', produced in the circuit with that name, gives a signal which is low five number times earlier than the phase and number time of the desired location. The conditions for the circuits m' and M-5' are shown in Figs. 3-13 and 3-14. The outputs m,..., m+4 are used in the delay line selection circuits.

States 2 to 4 of the control ring are used to introduce the delay which is required by the selection relays. The ring remains standing in state 4 until the output M-5' becomes low, and arrives in state 6 five number times later. During the remaining four states the transfer takes place. The ring is stepped from state 6 to state 7 during 18 digit time

of the number time during which the first number is to be read. It stays in state 7 for five number times, after which it is stepped during 10 digit time to state 8 and during the following 18 digit time to state 9. This marks the end of the transfer of the first five numbers. At the end of the transfer of the next five numbers the ring is again stepped twice and returns to the home position. The output SR4' is low during the entire transfer. This output is used in the pulse selection circuit, and also, together with the outputs SR3 and SR3', in the delay line gating circuits. The output SRH, obtained from the outputs of the ring, is high when the ring is home. This output is used to reset the triplet ST and the trigger pairs SS200, SS210 and SSRR. The output is also used in the Wait circuit of the sequence mechanism to indicate the time during which the Slow Storage Unit is busy.

The three states of the triplet ST are shown in Table 3-4,

Table 3-4

ST	3	2	1		
1)	0	0	1	4P'; 4NT'; 17DT'; SR4'; (II-III); (I-II) → 2	↺
2)	0	1	0	1P'; 1NT'; 10DT'; ST1 → 3	
3)	1	0	0	SS200; SS210 → 1	

together with the conditions which control the change from one state to the next. The output ST1 is high when the triplet is in its home position.

The operation of the triplet is threefold: a) The triplet will reset the trigger pair SR4 to the state where the output SR4' is high. This is controlled by state 2 of the triplet. SR4' is reset at the beginning of 0 P, 0 NT. b) The triplet will control the relay selection circuit in

such a way that the relay which was selected is dropped out and the next relay is picked up. This was described in Part C. c) After the triplet has reached state 3 it will make the output SR4' low again during 0 P, 0 NT. The conditions for the triplet are shown in Fig. 3-15. Level 2 of the circuit for ST2 shows that the triplet will begin its cycle only when the control ring is in one of the states 7 - 10, that is, during a transfer. The control ring remains in either of the states 0100 or 0010 during the interposed drum revolution. At the end of this wait cycle, the ring cycling is resumed where it left off previously. The operation of the triplet adds twenty-five cycles to the time which is necessary for a transfer, and is required when the control number is in the range --91 to --99. On the average, these numbers will occur for only nine percent of the transfers. It is, moreover, expected that a large number of the control numbers will have a zero unit's digit, which will further reduce this percentage.

The conditions for the trigger pairs SS200, SS210 and SSRR are shown in Fig. 3-16. The trigger pairs store the information which is obtained from the sequence code initiating the transfer. The output SS200' is low when it is desired to transfer the registers S_0 - S_9. The transfer of the registers S_0' - S_9' is indicated by a low output SS210'. The outputs of these trigger pairs are used in the delay line selection circuits and in the Wait circuit of the Sequence Unit. A low output of SSRR' specifies a recording operation. SSRR is low in the case of a read operation. These outputs control the pulse selection circuit.

F. Pulse Selection

The pulse selection circuits are used: a) to select the pulses with which numbers will be recorded on the storage drum; b) to select the pulses which are used in reading numbers from the drum. The unit's and the ten's digits of the control number determine which pulse should be selected. The numbers 00-24 are recorded with the pulse B_1 and played back with the pulse A_1. The numbers 25-49, 50-74 and 75-99 use the pulses B_2, B_3, B_4 and A_2, A_3, A_4, respectively.

The selection of the proper pulse is performed in two stages. In the first stage the outputs (I - II) and (II - III) are obtained. Table 3-5 shows which pulses are selected for the four possible combinations of these outputs. In the second stage the outputs thus obtained are used to gate one of the four pulses B_1, B_2, B_3, and B_4. The gating circuit makes use of vacuum tube diodes (Fig. 3-17).

The conditions for the circuits (I - II) and (II - III) are shown in Fig. 3-18. Levels 2-5 of the circuit (I - II) show that the output (I-II)' will be low for a 0, 1, 2 or 3 in the ten's register of the Slow Storage Control Register. In addition, level 1 will be low when this register stores a 9 and the output $a+$ is low, and level 6 will be low for a 4 when the output $a-$ is low. The outputs $a-$ and $a+$ are obtained from the phase ring and will be low during 0 P, 1 P and part of 2 P, and during 3 P, 4 P and part of 2 P, respectively. Thus the output (I - II)' is low during the transfer to the number locations 00-49, and high during the transfer to number locations 50-99. This can be illustrated with an example. If the control number is 43, then the output (I - II)' will be low while the numbers 43-49 are transferred and high during the transfer to the number locations 50 to 52. Since (II - III)' is low during the

Table 3-5

(I-II)	(II-III)	Pulses selected	Number locations
1	0	A1, B1	00-24
1	1	A2, B2	25-49
0	1	A3, B3	50-74
0	0	A4, B4	75-99

entire transfer, B_2, will be selected for the first seven numbers and B_3 for the last three numbers. A similar switching operation is performed for the control numbers 15-24, 65-74 and 90-99.

Figure 3-17 shows that the B pulse which is selected by the diode circuit is switched under control of the outputs of SSRR. With SSRR' low in the case of a recording operation, the pulse is inverted twice and sent to the record units. The pulse is gated by the output SR4', so that the record pulses will be present only during the recording operation. The operation of the record circuits is controlled by the presence or absence of the record pulse. In the case of a read operation the output SSRR will be low. The pulse is delayed by means of a multivibrator and used in the playback circuits. The delayed B pulse is referred to as an A pulse.

G. Delay Line Selection

Figure 3-19 shows the schematic diagram of the selection circuits for the twenty delay lines associated with Slow Storage. These are identical to the Fast Storage delay lines. Each delay line is controlled by three signals: a) the gate signal, which is high when the delay line is to be advanced and which goes to -120 V when the delay line is not to be advanced; b) and c) the pulses D1 and D2 which are used in the advancing of the delay line. When the delay line is to be advanced the pulses D1 and D2 should be present as well as the gate signal. The gate signal and the pulses are provided by tubes which are controlled by selenium rectifier circuits. Examples of the conditions for the gates are shown in Fig. 3-20. The conditions for the control of the D1 and D2 pulses are shown in Fig. 3-21. Each of the selenium circuits can be controlled either from the sequence codes or from the Slow Storage timing signals. In addition to the controls for the delay line advance circuits, provision is made to switch the input and output cores of these delay lines between the Slow Storage and the Fast Storage part of the machine. These switching operations are performed by standard selenium rectifier circuits as is shown in Fig. 3-17. The conditions for these circuits are shown in Fig. 3-22. The playback, record and delay line circuits of Slow Storage will not be discussed in detail.

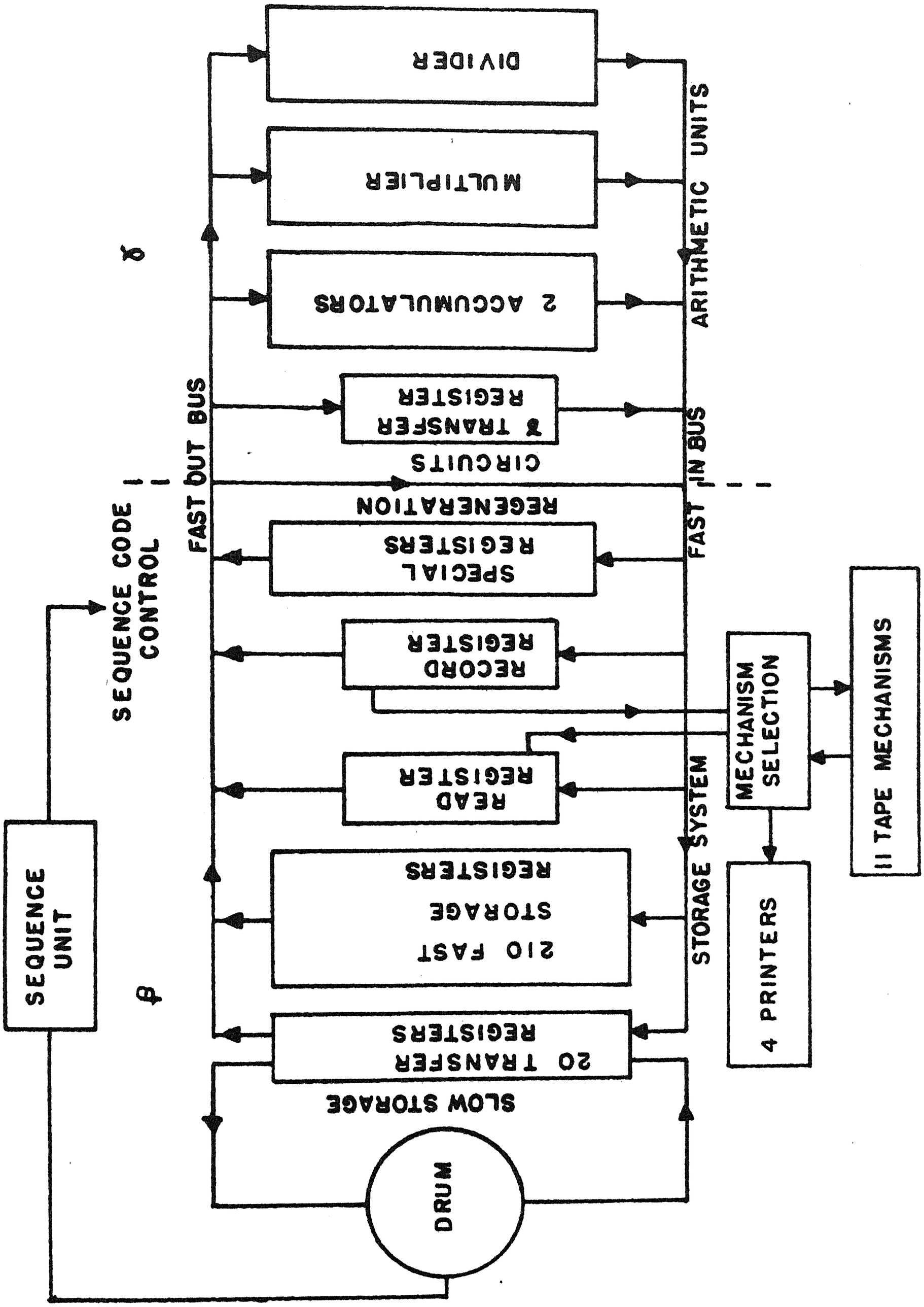


Fig. 3-1. Block Diagram of Mark IV

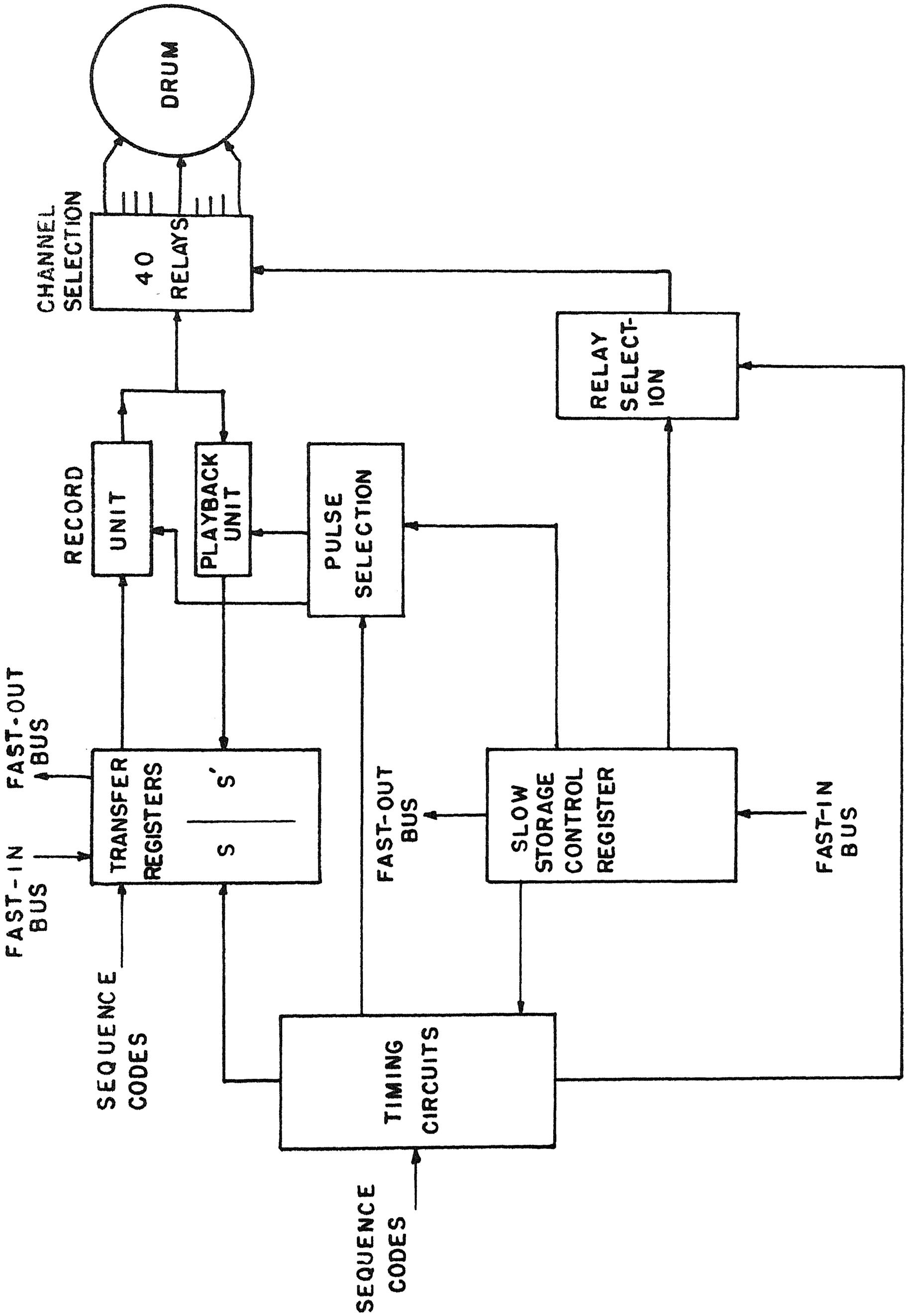


Fig. 3-2. Block Diagram of Slow Storage

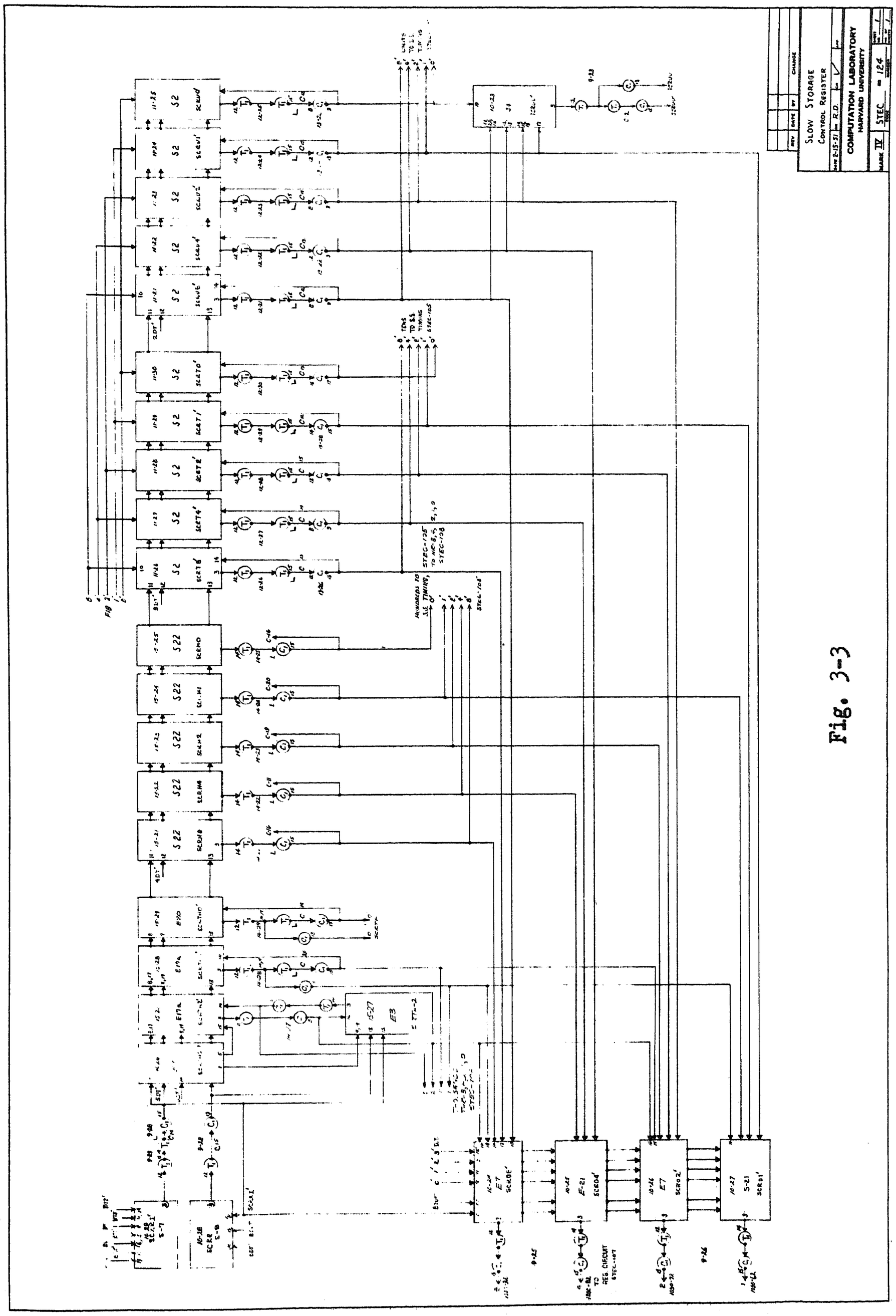

SLOW STORAGE
CONTROL REGISTER
COMPUTATION LABORATORY
HARVARD UNIVERSITY
SYEC - 124

Fig. 3-3

SCRRI' Type S7 STEC-124

1.	1201 S in	βH2'; 4	βT0'; 5	βU11' 6
2.	1211 S out	βH2'; 7	βT1'; 8	βU11' 9
3.	1221 S' in	βH2'; 10	βT2'; 11	βU11' 12
4.	1231 S' out	βH2'; 13	βT3'; 14	βU11' 15
5.	3200	βH2'; 16	βT10'; 17	βU10' 19

SCRR Type S9 STEC 124

1.	0 DT' 10	SCRRI'; 11	β Out 12

Fig. 3-4

SCRU-8' Type S2 STEC-124

1.	Reset	SCRR; 13	SCRU-8' 14	
2.	Read in	FIB8'; 10	SCRRI'; 11	2 DT' 12

SCRT-8' Type S2 STEC-124

1.	Reset	SCRR; 13	SCRT-8' 14	
2.	Read in	FIB8'; 10	SCRRI'; 11	3 DT' 12

SCRH-8' Type S22 STEC-124

1.	Read in	FIB8; 10	SCRRI'; 11	4 DT' 12	
2.	Hold 1	0'	1'		
3.	Hold 2	0'		2'	
4.	Hold 4	0'			4'
5.	Hold 6		1'	2'	
6.	Hold 0		1'		4'
7.	Hold 5			2'	4'

13 14 15 16

Fig. 3-5

SCRTH-2' Type E17

1. Hold	SCRTH-2' 14				
2. Change (5,7,9)	SCRRI'; 8	6 DT'; 9	SCRTH-0'; 10	FIB-1; 11	FIB-0 12
3. Change (1,3)	SCRRI'; 17	6 DT'; 19	SCRTH-0'; 16	SCRTH-2'A(5) 15	

SCRTH-2'A Type E9

3. Change	FIB-4; 8	FIB-2; 9	FIB-1' 10	
			Join SCRTH-2'A(5), SCRTH-2'(15)	

SCRTH-2 Type E3

1. Hold	SCRTH-2; 14	SCRR 13		
2. Read in (2,6,7)	SCRRI'; 12	5 DT'; 15	FIB-2'; 16	FIB-4 17
3. Read in (3)	SCRRI'; 12	5 DT'; 5	FIB-8'; 6	FIB-1' 7
4. Change (5,7,9)	SCRTH-2(6); 19	FIB-1; 20	FIB-0 18	
5. Change (1,3)	SCRTH-2(6); 9	FIB-4; 10	FIB-2; 11	FIB-1' 8

SCRTH-2A Type E9

4,5. Change	SCRRI'; 13	6 DT'; 14	SCRTH-0 15	
			Join SCRTH-2A(6), SCRTH-2(9,19)	

Fig. 3-6 (cont. on next page)

SCRTH-1' Type E17

1.	Hold	SCRRI'; 14	SCRR 13			
2.	Read in (2,4,8)	SCRRI'; 8	5 DT'; 9	FIB-0'; 10	FIB-1 11	
3.	Read in (0,6)	SCRRI'; 17	5 DT'; 19	FIB-1'; 15	FIB-0; 16	FIB-8 18

Fig. 3-6 (concluded)

SCRTH-0' Type E20

1.	Hold	SCRTH-0'; 14	SCRR 13	
2.	Read in	SCRRI'; 8	5 DT'; 9	SCRTH-2 10

Fig. 3-7

SCRO-8' Type E7

1.	Units	SCRRI'; 8	β Out'; 11	0 DT'; 9	SCRU-8' 10	
2.	Tens	SCRRI'; 7	β Out'; 6	1 DT'; 5	SCRT-8' 4	
3.	Hundreds	SCRRI'; 15	β Out'; 12	2 DT'; 13	SCRH-8' 14	
4.	Thousands	SCRRI'; 17	β Out'; 20	3 DT'; 16	SCRTH-2; 18	SCRTH-1 19

Fig. 3-8

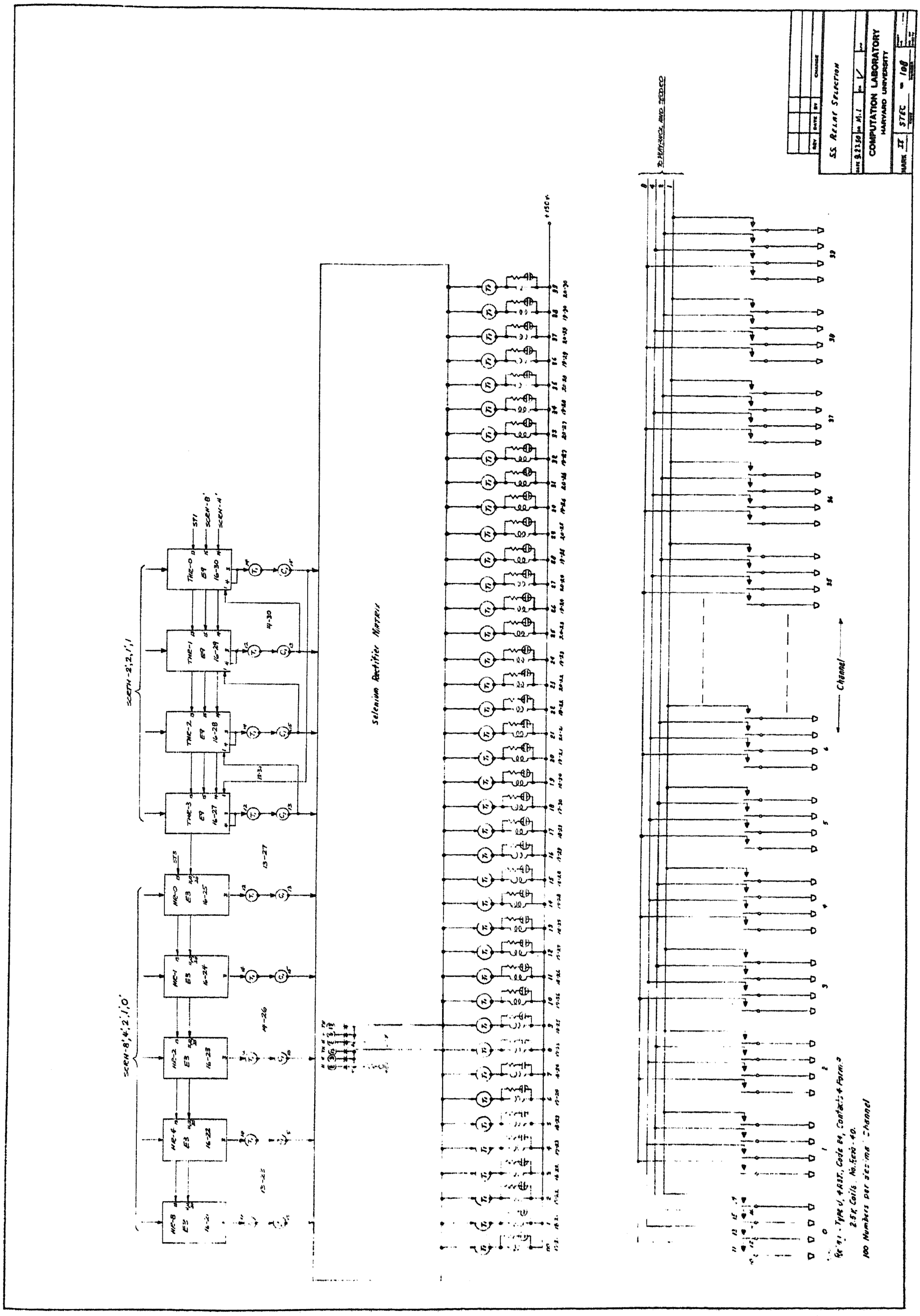

SS. Relay Selection
COMPUTATION LABORATORY
HARVARD UNIVERSITY
Selenium Rectifier Matrix
To Punches and Selco
Channel
Fig. 3-9 - Type G, 4 PDT, Code #4, Contacts 4 Form C
2.5K Coils, No. Sets 40.
100 Numbers per section - Channel

Fig. 3-9

HR2		Type E3		
1.	Regular	SCRH-2'; 14	ST3 13	
2.	Next relay (1)	SCRH-1'; 18	SCRH-0'; 19	ST1 20
3.	Next relay (4)	SCRH-4'; 8	SCRH-0'; 9	ST1 11
4.	Next relay (5)	SCRH-4'; 17	SCRH-2'; 16	ST1 12
5.	Next relay (6)	SCRH-2' 7	SCRH-1'; 6	ST1 12

THR1		Type E9				
1.	Regular	SCRTH-2'; 8	SCRTH-1 9			-45 V THR2 1
2.	Next relay	SCRTH-2'; 17	SCRTH-1'; 16	SCRH-8'; 15	SCRH-4'; 14	ST1 13

Fig. 3-10

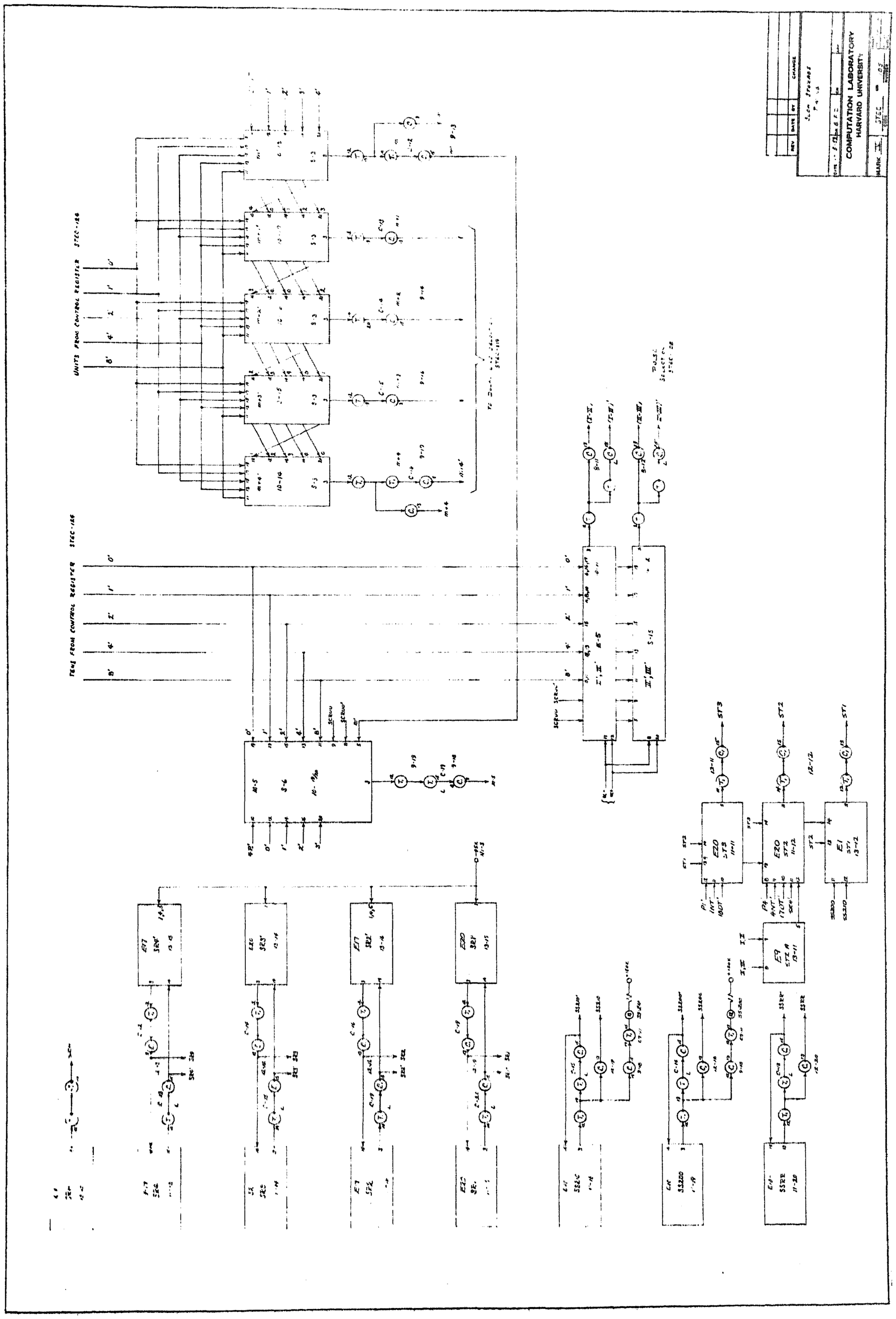

COMPUTATION LABORATORY
HARVARD UNIVERSITY
UNITS FROM CONTROL REGISTER STEC-126
TENS FROM CONTROL REGISTER STEC-126
PULSE STEC-28

Fig. 3-11

SR4	Type E17				STEC-105
1. Hold	SR4 14				
2.	18 DT'; 10	SR3; 11	SR1 12		
3.	18 DT'; 19	ST1; 18	ST3 17		

SR3	Type S2			STEC-105
1. Hold	SR3 14			
2.	18 DT'; 10	SR1; 11	SR2' 12	

SR2	Type E17				STEC-105
1. Hold	SR2 14				
2.	M-5'; 9	0 DT'; 10	SR4; 11	SR3' 12	
3.	10 DT'; 15	m+4'; 16	SR4'; 17	SR3 18	

SR1	Type E20					STEC-105
1. Hold	SR1 14					
2.	10 DT'; 8	m+4'; 9	SR4; 10	SR3'; 11	SR2 12	

Fig. 3-12 (cont. on next page)

SR4'	Type E17				STEC-105
1. Hold	SR4' 14				-45 V N1-3 1,4,5
2.	18 DT'; 10	SR3'; 11	SR1; 12	ST2; 8	ST3 9
3.	OP'; 15	0 NT'; 16	ST1; 17	ST2 18	

SR3'	Type E20				STEC-105
1. Hold	SR3' 14				-45 V N1-3 1
2.	2 DT'; 9	m'; 10	SR2'; 11	SR1' 12	

SR2'	Type E17				STEC-105
1.	SR2' 14				-45 V N1-3 1,4,5
2.	4 DT'; 8	m'; 9	SR4; 10	SR3; 11	SR1' 12
3.	10 DT'; 15	m+4'; 16	SR4'; 17	SR3' 18	

SR1'	Type E20				STEC-105
1. Hold	SR1' 14				-45 V N1-3 1
2. Start	SCRRI'; 8	SR4; 9	SR3; 10	βU11'; 11	ODT' 12

Fig. 3-12 (concluded)

m'		Type S3		
1.	9	SCRU-8'; 11	SCRU-4'; 13	4NT' 20
2.	4	SCRU-4'; 13	SCRU-0'; 19	4NT' 20
3.	8	SCRU-8'; 11	SCRU-0'; 19	3NT' 16
4.	3	SCRU-8'; 11	SCRU-1'; 17	3NT' 16
5.	7	SCRU-8'; 11	SCRU-2'; 15	2NT' 14
6.	2	SCRU-2'; 15	SCRU-0'; 19	2NT' 14
7.	6	SCRU-2'; 15	SCRU-1'; 17	1NT' 12
8.	1	SCRU-1'; 17	SCRU-0'; 19	1NT' 12
9.	5	SCRU-4'; 13	SCRU-2'; 15	ONT' 10
10.	0	SCRU-4'; 13	SCRU-1'; 17	ONT' 10

Fig. 3-13

M-5' Type S6 STEC-105

1.	00-04	SCRT-4'; 13	SCRT-1'; 17	SCRUU; 9	P4'; 10	m' 5
2.	25-29	SCRT-2'; 15	SCRT-0'; 19	SCRUU'; 8	"	"
3.	50-54	SCRT-4'; 13	SCRT-2'; 15	SCRUU; 9	"	"
4.	75-79	SCRT-8'; 11	SCRT-2'; 15	SCRUU'; 8	"	"
5.	05-09	SCRT-4'; 13	SCRT-1'; 17	SCRUU'; 8	PO'; 12	"
6.	30-34	SCRT-8'; 11	SCRT-1'; 17	SCRUU; 9	"	"
7.	55-59	SCRT-4'; 13	SCRT-2'; 15	SCRUU'; 8	"	"
8.	80-84	SCRT-8'; 11	SCRT-0'; 19	SCRUU; 9	"	"
9.	10-14	SCRT-1'; 17	SCRT-0'; 19	SCRUU; 9	P1'; 14	"
10.	35-39	SCRT-8'; 11	SCRT-1'; 17	SCRUU'; 8	"	"

Fig. 3-14 (cont. on next page)

M-5 (continued)

11.	60-64	SCRT-2'; 15	SCRT-1'; 17	SCRUU; 9	P1'; 14	m' 5
12.	85-89	SCRT-8'; 11	SCRT-0'; 19	SCRUU'; 8	"	"
13.	15-19	SCRT-1'; 17	SCRT-0'; 19	SCRUU'; 8	P2'; 16	"
14.	40-44	SCRT-4'; 13	SCRT-0'; 19	SCRUU; 9	"	"
15.	65-69	SCRT-2'; 15	SCRT-1'; 17	SCRUU'; 8	"	"
16.	90-94	SCRT-8'; 11	SCRT-4'; 13	SCRUU; 9	"	"
17.	20-24	SCRH-2'; 15	SCRH-0'; 19	SCRUU; 9	P3'; 20	"
18.	45-49	SCRH-4'; 13	SCRH-0'; 19	SCRUU'; 8	"	"
19.	70-74	SCRH-8'; 11	SCRH-2'; 15	SCRUU; 9	"	"
20.	95-99	SCRH-8'; 11	SCRH-4'; 13	SCRUU'; 8	"	"

Fig. 3-14 (concluded)

ST3 Type E20

1. Hold	ST1; 13	ST2 14			
2.	1P'; 12	1NT'; 11	10 DT'; 10	ST1 9	

ST2 Type E20

1. Hold	ST1; 13	ST3 14			
2.	4P'; 8	4NT'; 9	17 DT'; 10	SR4'; 11	ST2A(5) 12

ST2A Type E9

2.	(II-III); 8	(I-II) 9	Join ST2A(5), ST2(12)

ST1 Type E1

1. Hold	ST2; 13	ST3 14	
2.	SS200; 11	SS210 12	

Fig. 3-15

SS200'	Type E10			STEC-105
1. Read in S	SCRRI'; 10	βTO'; 11	10 DT' 12	
2. Read out S	SCRRI'; 7	βT1'; 8	10 DT' 9	
3. Hold	SS200'; 14	SRH 13		

SS210'	Type E10			STEC-105
1. Read in S'	SCRRI'; 10	βT2'; 11	10 DT' 12	
2. Read out S'	SCRRI'; 7	βT3'; 8	10 DT' 9	
3. Hold	SS210'; 14	SRH 13		

SSRR'	Type E10			STEC-105
1. Record from S (β1211)	SCRRI'; 10	βT1'; 11	10 DT' 12	
2. Record from S' (β1231)	SCRRI'; 7	βT3'; 8	10 DT' 9	
3. Hold	SSRR'; 14	SRH 13		

Fig. 3-16

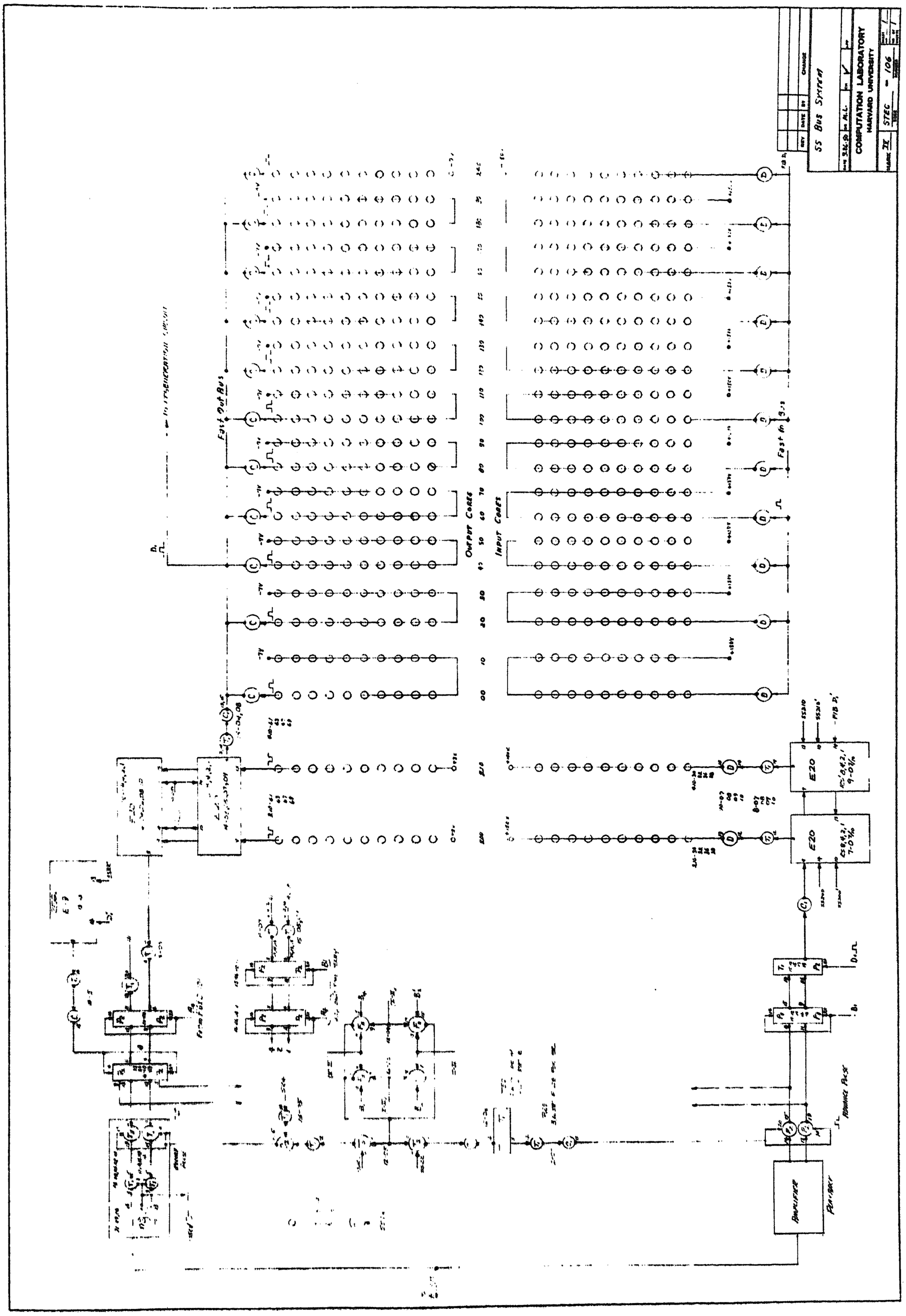

55 Bus System
COMPUTATION LABORATORY
HARVARD UNIVERSITY
STEC - 106
Fast Out Bus
Output Codes
Input Codes
Fast In Bus
E20
E20
Buffer
Printer

Fig. 3-17

(I-II)' Type E5

1.	90-99 a+	SCRT-8'; 11	SCRT-4'; 18	a+ 12	
2.	00-09	SCRT-4'; 13	SCRT-1' 14		
3.	10-19	SCRT-1'; 4	SCRT-0' 6		
4.	20-29	SCRT-2'; 15	SCRT-0' 16		
5.	30-39	SCRT-8'; 10	SCRT-1' 8		
6.	40-49 a-	SCRT-4'; 18	SCRT-0'; 19	a- 17	

(II-III)' Type S15

1.	40-49	SCRT-4'; 13	SCRT-0' 19		
2.	50-59	SCRT-4'; 13	SCRT-2' 15		
3.	60-64	SCRT-2'; 15	SCRT-1'; 17	SCRUU 5	
4.	65-69 a-	SCRT-2'; 15	SCRT-1'; 17	SCRUU'; 9	a- 8
5.	70-74 a-	SCRT-8'; 11	SCRT-2'; 15	SCRUU; 5	a- 8
6.	15-19 a+	SCRT-1'; 17	SCRT-0'; 19	SCRUU'; 9	a+ 20
7.	20-24 a+	SCRT-2'; 15	SCRT-0'; 19	SCRUU; 5	a+ 20
8.	25-29	SCRT-2'; 15	SCRT-0'; 19	SCRUU' 9	
9.	30-39	SCRT-8'; 11	SCRT-1' 17		

Fig. 3-18

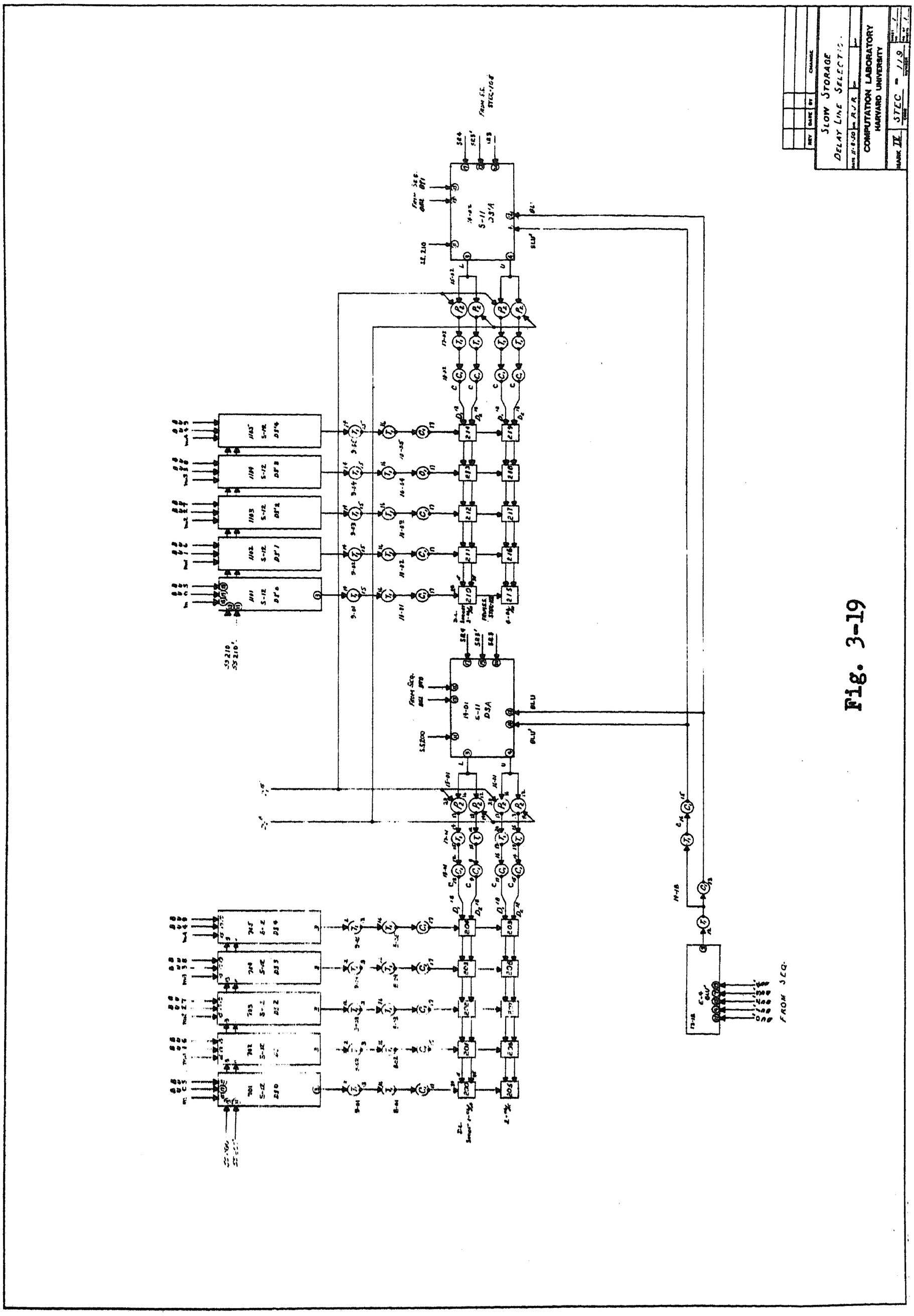

SLOW STORAGE
DELAY LINE SELECTION
COMPUTATION LABORATORY
HARVARD UNIVERSITY
MARK IV
FROM SEQ.

Fig. 3-19

DSO	Type S12			STEC-119
1.	SS200; 13	m 15		
2.	SS200'; 11	βU0 17		
3.	SS200'; 11	βU5 19		Positive sensing card

DS'2	Type S12			STEC-119
1.	SS210; 13	m+2 15		
2.	SS210'; 11	βU2 17		
3.	SS210'; 11	βU7 19		Positive sensing card

Fig. 3-20

DSL	Type S11 (out 3)				STEC-119
1.	SS200; 11	SR3; 20	SR4 17		
2.	βLU; 12	βH2; 13	βT0 15		Positive sensing card

DSU	Type S11 (out 4)			
1.	SS200; 11	SR4; 17	SR3' 19	
2.	βLU'; 14	βH2; 13	βT0 15	Positive sensing card

Fig. 3-21

OD-8	Type E20		
1.		SS200; 14	S'8 13
2.		SS210; 10	S8 9
OS-8	Type E20		
1.		SS210; 14	S'8 13
2.		SS200; 10	S8 9
RS-8	Type E20		
1.	FIB	FIB-8'; 13	SS200 14
2.	Slow Storage	SIB-8'; 9	SS200' 10
RS'-8	Type E20		
1.	FIB	FIB-8'; 14	SS210 13
2.	Slow Storage	SIB-8'; 9	SS210' 10

Fig. 3-22

CHAPTER 4

SEQUENCE UNIT OF MARK IV

A. Introduction

In the sequence unit for Mark IV the majority of the switching operations is performed by selenium rectifier circuits. In the diagrams illustrating this chapter, such as Fig. 4-27, each selenium circuit is represented by a rectangle. The inputs to the selenium circuits are shown as arrows with their socket terminal points indicated inside the rectangle. In some cases, in the interest of clarity, only those inputs essential for this discussion have been shown. The output terminal, usually terminal 3, is indicated in a similar fashion. The abbreviated name of the circuit, the type of selenium circuit used, and the location of its socket in the machine are also given inside the rectangle. According to the logical convention used, the output of a circuit is designated unprimed when the desired output signal is high, and the output is designated primed when the desired output signal is low.

When it has been necessary or desirable, in particular cases, to join two or more standard selenium circuits together by external jumpers, each selenium circuit has been drawn separately, and the necessary jumper connections indicated. The representation of selenium circuits in this block form has been found more satisfactory than the use of a full schematic for each individual selenium circuit. Because of their construction, the selenium circuits are often called "cards." Details of the electrical operation of different types of cards are indicated on the drawings at the end of this chapter. For each card in the machine, a separate sheet specifies the logical or switching operations performed by the card, but

only those sheets required for the understanding of the operation of the sequence mechanism have been included here. Figure 4-37 shows one of these sheets. The name of the circuit (JCTR in this example) is given in the upper left corner. This name also identifies the circuit on the schematic diagram, as in the diagram SMEC-104, shown in Fig. 4-27. To the right on the same line as the name, "Type E17" designates the type of card used and "SMEC-104" refers to the schematic in which this circuit is incorporated.

All selenium circuits consist of one of more first levels tied together by one second level. A first level consists of several rectifiers connected to a common lead in a manner such that if and only if all the inputs to these rectifiers are low, the output of the level will be low. The connections to the second level are such that if one or more of the first level outputs is low, the second level output is low. This is the final output of the card. The inputs to each first level are indicated in the sheets on a horizontal line. Each line corresponding to a separate first level is numbered and has been given a name. The inputs to the rectifiers are listed by their abbreviated names, and their socket terminal points given below each. It is not necessary to provide a signal at each input of the selenium card. If at least one input of each level is used, no special precautions need be taken, but if a whole level is left blank, at least one input should be connected to a constant +3 V. Throughout the sequence unit all cards have been chosen so that no extra first levels occur. This avoids the introduction of a constant +3 V source. While the input signals of the cards are usually provided by cathode followers, when relays are used it is convenient to connect the -45 V supply terminal of the desired level or of the entire card through the relay to either -45 V or ground. When the supply terminal is at -45 V the card operates in

normal fashion. With the supply terminal connected to ground, the output of the level or card will be high regardless of its input signals.

In Fig. 4-37 all three available first levels of type E17 are used. Of first level 1, however, only four of five inputs are employed. The output of the circuit will be low if the signals JCTR', IJKR, 17DT, and 11DT are low at the same time, or if the signals DRUM' and 19DT' are low at the same time, or if all inputs to level 3 are simultaneously low. Note that level 3 has an input through relay contacts X1-3, M2-4' or K1-4', hence the considerations outlined above for such cases apply to this level. The kind of sheet shown in Fig. 4-37 is a simplified sample of a complete set of sheets which fully describe the sequence mechanism. The information on the complete sheets is used in the construction, testing and maintenance of the sequence mechanism.

B. General Organization

The functions of the sequence unit are the following:

1) to read in succession each of the ten thousand commands stored on the sequence drum, so that they may successively control the operation of the calculator;

2) to introduce a wait, and thereby prevent the occurrence of conflicting codes. A wait is introduced when the slow-fast storage transfer is in operation and there is a call for another transfer or for a read-out from one of the registers which is engaged in the transfer. A wait also is introduced when a read or record code occurs while the tape units are still engaged in the reading or recording operation;

3) to make the appropriate substitution in i, j, or k β-codes under control of the I, J and K Registers;

4) to change a conditional call code into a call code under control of the Condition Register;

5) to read the number introduced by an external transfer code into the γ Transfer Register;

6) to interrupt, in case of a call, the succession of codes read in numerical order and to start a new series beginning at the number read to the Line Number Register;

7) to record codes on the sequence section of the drum from any tape mechanism;

8) to provide manual controls to allow for: a) reading numbers into the machine, b) reading any number in the machine into indicators on the front of the machine, c) starting the operation of the machine at any desired line of coding, or at the line of coding following the line where the machine previously stopped, d) performing any desired code as stored

on the sequence drum, e) reading any such code without performing it, f) recording any code in any position on the drum, g) operating any code during one cycle, h) operating any code repeatedly for test purposes, i) stopping the machine immediately or at any desired line.

Figure 4-1 shows in a block diagram the inter-relation of the main units of the sequence mechanism. The Line Number Register (LNR) stores at each moment the line number of the code which is being performed, or in case the machine is stopped, the line number of the last code performed. In case of a call it is possible to read into the Line Number Register from the Fast In-Bus (FIB). Also, a read-out to the Fast Out-Bus (FOB) is available. During normal operation, the Line Number Register accumulates numbers and runs in succession through the numbers 0000-9999. It does so in part through internal cycling, and in part through information obtained from the drum, the pulse selection circuit, and the phase selection circuit (P*). From the drum the number time (NT) is obtained; from the pulse selection, the quadrant Q and odd/even output E. The phase selection is determined by the pole piece selection (PP), and the phase (P) from the drum. In turn, the Line Number Register controls the sequence gates and record relays which select one out of the five hundred pole pieces around the circumference of the storage drum. The Line Number Register also controls the pulse selection. The pulse selection selects one out of four advance or record pulses, which are used in the sequence playback and the sequence record units. It also provides the control for switching between the odd and even playbacks. The codes thus are read from the drum through associated gates to the playback, amplified and read into the First Sequence Trigger Pairs (FSTP). In a recording operation, the code is read from the First Sequence Trigger Pairs (FSTP) through the record unit and the record

relays onto the drum. The codes are read serially into the First Sequence Trigger Pairs and advanced in parallel into the Second Sequence Trigger Pairs (SSTP). A code with IJK control is changed to the desired code under control of the IJK Registers, while standing in the First Sequence Trigger Pairs. In similar fashion a conditional call code is changed to a call code under control of the Condition Register. The First Sequence Trigger Pairs also have a read-in from the Fast In-Bus (FIB) which is used for manual control and in the recording operations. The First Sequence Trigger Pairs have an output to the γ Transfer Register through the external transfer circuit. In addition, both the Line Number Register and First Sequence Trigger Pairs have an output to the line number and code indicators. Wait, call, stop, and manual operations are all performed through the Main Control Ring (MCR).

Figure 4-2 shows the layout of the Main Control Panel. The Read-In Switch (RIS) is at the top of this panel. A standard sixteen decimal digit number with its sign can be read from this switch into any β or γ register under control of a sequence command.

The number which is transferred under control of the code placed in the First Sequence Trigger Pairs can be displayed in the indicators above the Main Control Panel by means of the Number button. There are two indicators, each capable of displaying a sixteen-digit number and its sign (see Fig. 4-3). The toggle switch marked "Upper-Lower" provides a choice between the upper and the lower set of indicators. The indicator not controlled by the sequence mechanism can be used for reading numbers manually from any tape mechanism. To make it possible to reset the indicators a "Reset" button is available, which returns the indicators to their blank position. The toggle switch marked "Sign" is a manually

controlled register which can store a sign. The positive sign can be used in the case of a ganged number to indicate that the decimal point is located in the upper sixteen digits of the number, the negative sign indicating the opposite case. The seventeen-position strip switch marked "Decimal Point" provides for selection of the operating decimal point (O.D.P.) for the machine. Both the Sign and the Decimal Point can be read out onto the Fast Out-Bus. The decimal point is indicated by a number corresponding to the number of digits to the right of the decimal point.

The Go and Stop lights indicate whether the machine is running or not. When the machine is running, the Wait light comes on whenever a wait is introduced. The operation of the machine can be started either on a "specified line" or on a "next line," by use of the appropriate Start button. The specified line is placed in the Start Line Number (SAL) strip switches. The next line is the line following the one whose number is in the line number indicator. To operate the machine one cycle at a time, a One Line button can be used. Such a button is available to perform either a specified line or the next line and causes the number and the code of the line which has been performed to be displayed in an indicator. If it is desired to display the code and the line number without operation, the corresponding Read button can be used. The Stop button will stop the machine on whatever happens to be the next line. The toggle switch marked "Stop" will stop the machine whenever it has performed the line placed in the Stop Line Number (SOL) strip switches. The machine will stop either when a) the stop button is pushed; b) the specified stop line is reached; c) a stop code or a check code succeeds, or d) in case of an alarm. Whenever the machine stops, the last line which has been performed appears in the indicator, and an alarm bell sounds. It is necessary to push the button

marked "Bell" in order to stop this alarm. The toggle switch marked "Indicators" makes it possible to prevent the operation of the indicators for the line number and the code. There is a one-to-one correspondence between the number and the code displayed in the indicators and the number and the code available in the Line Number Register and the First Sequence Trigger Pairs respectively. When the machine is stopped, the line number and code can be read at any time to the indicators, by pushing the Stop button. By means of the set of buttons marked "Line Number" and "Code" it is possible to read numbers manually into the Line Number Register and to the First Sequence Trigger Pairs. In this operation the Line Number button must be pushed four times to write a four-digit number while the Code button must be pushed eight times to write a complete code, after which the new line number or the new code will appear in the indicators.

Whatever code is available in the indicator can be performed for one cycle by pushing the Operate button. It should be noted that the number held in the indicator may have an i, j or k control. When the code is being operated, this control is replaced by the numbers stored in the I, J or K Register. The code which has been operated is displayed in the indicator. For testing purposes, it may be desirable to perform repeatedly without any i, j or k control a code placed in the First Sequence Trigger Pairs. This may be done by pushing the Repeat button. The repeat operation is stopped as soon as any other button is pushed. A light indicates when a code is being performed repeatedly. The code displayed in the code indicator can be recorded by means of the Record button in the position on the drum corresponding to the number in the line number indicator. The Reset button is used to reset the line number and code indicators. Also, if the reading in of a line number or a code has not yet been completed,

the Reset button makes it possible to start over with the operation. The buttons to the right marked "Sequence Tape" are used for the reading of the codes from a regular tape mechanism. A code and associated line number can be read from the tape into the indicators under control of the pushbutton marked "Read." The codes and line numbers are recorded on the sequence tape, each line number being followed by its associated code. When the Run button is pushed the line numbers and codes are read in succession, but not displayed in the indicators. The operation can be stopped either by means of the Stop button, or under control of the stop line number. This allows the sequence mechanism to position to any line number on the tape. The Record button operates in a similar fashion but, in addition, the codes read from the tape are recorded onto the drum. The three buttons marked "Spare Mechanism" are associated with the tape mechanisms. They make it possible to read numbers from the spare tape mechanism into the indicators. This system has no circuit in common with the sequence mechanism and may be operated while the machine is running.

Figure 4-3 shows that provision has been made for twenty-two indicator lights. The lights used in connection with the sequence unit are:

a) Test Light: indicates that one or more of the six test switches located on the frame is in the "on" position. All test switches should be off during normal operation.

b) Incomplete Pole Piece Light: indicates that the number of pole pieces from which the codes can be read has been reduced. The machine runs less efficiently under this circumstance.

c) Incomplete Number Light: goes on if not all columns of the Read-In Switch (RIS) or Stop Line Number (SOL) have been pushed.

d) Condition Register Light: goes on when the Condition Register stores a negative sign.

e) External Transfer Light: goes on when an external transfer code is present in the First Sequence Trigger Pairs.

f) Line Number Light: indicates that a manual read-in of the line number is incomplete.

g) Code Light: indicates that a manual read-in of the code is incomplete.

h) Busy Light: goes on whenever the machine is performing an operation. No new operation can be started until the previous operation is completed.

A detailed description of each of the units mentioned above is given in the following parts.

C. Line Number Register

Figure 4.4 shows a schematic diagram of the Line Number Register (LNR) and auxiliary equipment. The Line Number Register can store numbers in the range 0000-9999. The unit's digits are stored in the five trigger pairs shown to the left and marked LNRU. The ten's digits are stored in the next five trigger pairs marked LNRT. The unit's and ten's digits are stored in the 84210 number system shown in Table 4-1. For the hundred's

Table 4-1

84210 (5C2) Code Used in LNR

	8 4 2 1 0 *
0	0 1 0 1 0
1	0 0 0 1 1
2	0 0 1 0 1
3	1 0 0 1 0
4	0 1 0 0 1
5	0 1 1 0 0
6	0 0 1 1 0
7	1 0 1 0 0
8	1 0 0 0 1
9	1 1 0 0 0

* Since only 8, 4, 2 and 1 resemble pure binary numbers, this way of naming the columns should not be mistaken for weighting.

and thousand's digits, two sets of trigger pairs are available. One set consists of the odd hundred's and thousand's registers, LNRHO and LNRTHO, and the other, of the even hundred's and thousand's registers, LNRHE and LNRTHE. The odd registers are used to control the odd sequence gates and the even registers to control the even sequence gates. The gates connect the drum channels with the sequence playbacks. Two sets of gates are used in order to allow fast switching between adjacent tracks. The outputs

of the odd and even playbacks are so switched that either the odd or the even gates may be used in the reading of codes. The set which is not actually reading may be switched from the track previous to the one being read, to the following track. The switching of the gates is performed immediately after the outputs of the playbacks have been switched. In normal operation the non-operative set of gates is connected to the track immediately following the track being read. As a consequence, the numbers stored in the odd and even registers differ by one. The odd hundred's are stored in the five trigger pairs LNRHO, the even hundred's in LNRHE. The outputs of the odd hundred's register are marked 1', 3', 5', 7' and 9', the outputs of the even hundred's register, 0', 2', 4', 6' and 8'. One and only one of the five outputs is low in each of the two sets of five trigger pairs, thus using a 5C1 number system. In one set, this is the output corresponding to the operating hundred's digit and in the other set the output corresponding to one higher than the operating hundred's digit. The numbers stored in the trigger pairs LNRTHO and LNRTHE are called the odd and even thousand's digits respectively. They are the thousand's digits corresponding to the odd and even hundred's digits. Usually, the odd and even thousand's registers store the same number. However, when the hundred's digit is nine the even thousand's register stores a number one higher than the number in the odd thousand's register. The numbers are stored in the thousand's registers using the 84210 number system. Figure 4-5 shows an example of the outputs of the trigger pairs, a) on the number 1234, and b) on the number 2987 stored in the Line Number Register.

The twenty-nine trigger pairs which form the Line Number Register are all of the three-grid type. A cathode follower has been added to fourteen of these trigger pairs in order to make the unprimed output available.

The resets for the register are provided for the unit's and ten's by the circuit R, for the odd hundred's and thousand's by the circuit RO, for the even hundred's by REH, and for the even thousand's by RETH. The logical characteristics of these circuits are shown in Fig. 4-6. The reset operates both when a new number is read in from the Fast In-Bus and when the internal cycling of the Line Number Register requires a change in the number stored. The reading in from the bus is controlled by the circuits LNRRI' and LNRRI'A, whose logical characteristics are shown in Fig. 4-7. These circuits are of the type mentioned in Part A of this chapter, where two cards are joined by external jumpers, the suffix "A" indicating the second card. The internal cycling is controlled either by the GO' circuit (Fig. 4-64) for the unit's and ten's digits, or by the add one (AO') circuit for the hundred's and thousand's digits. Figure 4-7 shows the specifications of circuits AO' and LNR 99. The circuit LNR 99 is used as an intermediate circuit to simplify the conditions for the reset and other circuits.

A line number is read from the Fast In-Bus without transformation into the unit's, ten's, and both thousand's registers. The hundred's digit is read into only one of the ten available trigger pairs. Thus after this read-in operation, the add-one operation has to be performed for the hundred's and even thousand's in order to put the Line Number Register in the desired state described above.

Figure 4-8 shows the sequence of operations under a normal call occurring on line 1234, when the line number to be read in is 2987. It should be noted that the first digit of a number appears at the Fast In-Bus at 2 digit time (Fig. 4-16).

The internal cycling of the Line Number Register consists of

adding unity to the number in the register for each cycle performed when the machine is running. In cycling, two different systems are used: for the unit's and ten's registers, the successive numbers are read in from information obtained from the basic cycling rings and the pulse and pole piece selection of the sequence unit. For the hundred's and thousand's registers, no such information is available, so that the numbers must be accumulated by cycling between the odd and even units.

Twenty-five codes are stored around the circumference of the drum in a single track and controlled by a single advance and record pulse. Since four advance pulses and corresponding record pulses are available, a total of one hundred codes can be stored on a single track, by using an interlacing scheme. The position of a code on the track is identified by the number time (NT) and the phase (P). There are five separate number times, 0 NT - 4 NT. Five successive number times form a phase and altogether five phases are available. In this way a position around the circumference of the drum is identified by the two variables NT and P, each of which can take on values 0 to 4. The rings from which these outputs are obtained are shown in Fig. 4-78.

The codes can be read from any one of five sets of pole pieces equally spaced around a track. In Fig. 4-4 the trigger pairs which select one out of the five sets of pole pieces around the circumference are marked PP0' - PP4'. The pole pieces are five number times, that is, one phase, apart in time. In order to determine the number of a code which is being read, it is necessary not only to know its number time and phase, but also the pole piece from which it is read. The pole piece selection and the operating phase (P) are combined in the circuits P*0' - P*4' shown in Fig. 4-4, so that each code location on the drum is identified by the number

time and P*. These outputs are used to read the number of the code which is performed into the unit's and ten's trigger pairs of the Line Number Register. Since these two outputs only identify one out of twenty-five codes, additional information has to be available to specify the group of twenty-five codes being read. This is obtained from the trigger pairs QI' and QII', as shown in Fig. 4-9. These trigger pairs are used for the advance and record pulse selection as will be described later. Their outputs and the corresponding decimal number are shown in Fig. 4-10.

The information available in terms of NT, P*, QI and QII is read into the unit's and ten's trigger pairs with a suitable translation. To reduce the number of rectifiers which is necessary to perform the translation an auxiliary output, DRUMLU, is obtained in the circuit DRUMLU (Fig. 4-11). An example of the selenium circuits used is shown in Fig. 4-12, which describes the selection of LNRU2'. Level 1 of this circuit serves to hold the trigger pair and to reset it under control of the signal R. Read-in from the Fast-In Bus (FIB) is performed by level 2 under control of LNRRI', at 2 digit time. During 16 digit time levels 3-5 take care of reading in the number of the next line, as defined by the signals NT' and DRUMLU. Reading in is performed only while the machine is running and the signal GO' is low. When the machine is stopped, or when a call or wait is performed, the signal GO' is high.

In every cycle, both the unit's and the ten's registers are reset, and the next line number is read in from the outputs which have been described above. The hundred's and thousand's combination has to be increased by 1 only once in every one hundred codes when the unit's and ten's read 99. This corresponds to a switch from the odd gates to the even gates. This switch is performed under control of the trigger pair E2 as shown in Fig. 4-9.

Figure 4-10 shows that when the odd sequence gates are in control, the output E2 is low, and when the even gates are in control the output E2' is low. Within the first number time in which the even gates are in control the odd trigger pairs are changed from the last hundred's and thousand's number to a number which is two higher. This is done by reading the outputs of the even hundred's into the odd hundred's selection circuit. For example, if the even hundred's trigger pair 4 is low, the odd hundred's trigger pair 5 will be selected. This selection is preceded by a reset. Both the odd hundred's trigger pairs and thousand's trigger pairs are set at the same moment. The odd thousand's digit read in will be identical to the even thousand's digit with the even gates in control. The even trigger pairs are reset during the cycle in which the unit's and ten's read 99 and the odd gates are in control. For the even hundred's digit the operation is similar to that described for the odd hundred's digit. For the thousand's digit, a reset and read-in will occur only when the odd hundred's digit is 9. In reading in, a translation is performed in which the even thousand's register adds one to the number stored in the odd thousand's register. For example, in Fig. 4-13, the selection conditions for the trigger pair LNRTHE4' are shown. Level 1 is the hold level which can be reset by the signal RETH. The read-in from the bus is performed through level 2 at 5 digit time under control of LNRRI'. In the add-one operation, LNRTHE4' should be low when the even thousand's register reads 0, 4, 5 or 9. At the time of switching, the odd thousand's register reads 9, 3, 4 or 8 depending on the number in the even thousand's register. Level 3 will be low under control of AOE' and LNRHO-9' when the odd thousand's digit is 3, 8 or 9. Level 4 is a second hold level which will keep the output of the circuit low when LNRTHO-0' is low. This occurs together with LNRTHE-4' only for the change from 4 to 5.

A code must be read out from the drum one number time before it is to be performed under control of the Second Sequence Trigger Pairs. Figure 4-14 shows a section of a timing diagram describing the moment at which the different switching operations are performed. Lines 1 and 2 show the number time (NT) and phase (P*) as obtained from the timing rings. Line 3 shows the unit's and ten's digits of the number of the stored code. The storage of code 99 begins one digit time earlier than number time 4, phase 4. Between codes 99 and 0 the outputs QI and QII, as well as E2, change at 17 digit time. Line 4 shows the number of the operating code. When called or reached in turn, code 99 acts during phase 0, number time 0, beginning at 18 digit time. At that time the Line Number Register should hold the number 99. In order to translate conveniently the number time and phase into the number 99, it is desirable that the Line Number Register change the number stored in it during 11-16 digit times of the previous cycle. The line number is consequently available from 17 digit time to 10 digit time and in a state of transition from 11-16 digit time. Reset of unit's and ten's occurs at 15 digit time and read-in at 16 digit time. In case unit's and ten's read 99, at 11 digit time the non-operating hundred's and thousand's are reset and the add-one operation is performed at 14 digit time. The timing for the transition of the number 9999 to the number 0000 is shown in Fig. 4-15.

D. Pulse and Pole Piece Selection

In this part, the pulse selection circuit for the sequence playback and record circuits will be described together with the matching circuit and pole piece selection. Figure 4-9 shows the majority of the circuits involved. Signals are obtained from the sequence drum through both the odd and even sets of gates. They are amplified and read through pentode gates into output trigger pairs. These gates are controlled by advance pulses. The selection of one out of four advance pulses is made by hard diodes symbolically represented as F_3. The circuit requires the coincidence of a negative advance pulse with the outputs of the circuits QI and QII, so that if all three voltages applied to F_3 are negative, the output will be negative also. This output is amplified, consequently delayed and inverted, and then sent to the pentode gate. The signal played back at the same time as the desired advance pulse will be advanced into the output trigger pairs. From these trigger pairs the signal is advanced by a B_1 pulse into the final triode trigger pair. Only one of the two output trigger pairs is advanced this way, its selection being determined by the output of the E2 selenium circuit. The cathode follower output of the triode trigger pair reads into the First Sequence Trigger Pairs, under control of a GO' signal obtained from the Main Control Ring. The signal thus delivered to the First Sequence Trigger Pairs is called DRUM'. QI, QII and E2 are four grid trigger pairs, whose outputs are shown in Fig. 4-10.

The sheets for the trigger pair QI-QI' are shown in Fig. 4-17; those for QII-QII' are shown in Fig. 4-18. In each circuit first level 1 is used for holding. The other first levels are used to set the trigger pairs to the desired state on reading in, under control of MCR3' and MCR4', and to change the output of the trigger pairs when the machine is running

and the Line Number Register reads 24, 49, 74 or 99. The latter operation is performed under control of the signal GO'. This signal is included in the auxiliary output LNR99'.

Figure 4-19 shows the logical specifications for the trigger pair E2-E2' and its auxiliary circuit E1'. The output E1' is low whenever the hundred's digit of the number stored in the Line Number Register is even. For the trigger pair E2-E2', level 1 is again the holding level, the other levels perform the read-in under control of the signals LNRRI', MCR3' and MCR4', and the change-over when the unit's and ten's read 99 and the machine is running.

In the recording operation the line number and the code are read from the Fast In-Bus into the Line Number Register and the First Sequence Trigger Pairs, respectively. This operation will be discussed in the part describing the Main Control Ring (Part J). The trigger pairs QI and QII again determine the pulse selected. The record pulse is sent through a pentode gate to the record unit. This gate, controlled by a four-position ring, allows the record pulses to be fed into the record unit during exactly one number time. Since no gap is available, this switching operation must be performed in eight microseconds. For this reason, the ring of four was introduced. The code digits to be recorded are combined in the selenium circuit REC with the appropriate digit time and sent in serial order into the record trigger pair under control of an A_4 timing pulse. A relay selection circuit connects the record unit to the desired pole piece (Fig. 4-20). Figure 4-21 shows the sections into which the drum surface is divided. The five large sections P0, P1..., P4, are each subdivided into five sections NT0, NT1,..., NT4. The operating phase and number time are determined by the drum section read by the pole piece set I. In the

example of Fig. 4-21 these are P1 and NT4, respectively. It can be seen that each of the five pole piece sets reads the same number time. The drum section read by the operating sequence pole piece set determines the output P*. In the given example, if pole piece set IV is reading, the output P*4 will be low. If an A_3 advance pulse is used, code --74 is being read and the code --73 is operating at the moment shown in the figure. Only one of the five sets of pole pieces around the circumference is used for recording. It is the set marked "I" on Fig. 4-21.

The circuits to the right in Fig. 4-9 provide a match between the number in the Line Number Register and the timing of the drum. They are used to provide the timing for the record operation and for the starting of the reading of sequence commands. In order to provide a sufficient time delay for switching the class A Gates, the number in the Line Number Register is matched with the number time (NT) and the phase (P*) in such a fashion that the match occurs four number times before the code corresponding to the number in the Line Number Register is to operate. In the regular cycling operation, the line number is read into the Line Number Register at the end of the cycle preceding the one during which the corresponding code is to operate (Fig. 4-14). Compared to the reading-in of the number time and phase to the Line Number Register, a shift of only three number times between the number standing in the Line Number Register and its corresponding number time and phase is necessary. This requires a match between the number time and phase and a number three less than the number standing in the Line Number Register. This match is accomplished by the circuits m-3, M-3, LNRLU and LNRMU.

The circuit m-3, whose logical characteristics are shown in Fig. 4-24, matches the unit's digit of the number in the Line Number Register

with a number time three less than this digit (modulo 5). Thus unit's digit 0 matches with 2 number time rather than with 0 number time, and unit's digit 1 with 3 number time instead of 1 number time. Similarly unit's digit 5 matches with 2 number time, and unit's digit 6 with 3 number time, and so on. A low output of the circuit m-3 indicates that the number time is properly matched with the number in the Line Number Register. The output of m-3 is combined with the output of M-3 in a double triode, a low output of M-3 indicating that the phase has been matched properly.

Figure 4-25 shows the sheet for M-3. Phase 0 (P*0) should match with the decimal numbers 03-07, 28-32, 53-57 and 78-82. These numbers are three more than the numbers 00-04, 25-29, 50-54 and 75-79, respectively, which would occur in a direct match. In order to obtain these numbers in a simple fashion from the outputs of the Line Number Register, the two auxiliary circuits LNRLU and LNRMU have been introduced. The sheets for these circuits are shown in Figs. 4-22 and 4-23 respectively. The output of LNRLU is low for the lower five unit's digits, 0-4. The output of LNRMU is low for the unit's digits 3-7. The outputs of these two circuits taken together make it possible to divide up the unit's digits into the three groups 0-2, 3-7 and 8-9, which are necessary for the match with the phase, P*. Figure 4-25 shows that a total of fifteen first levels are necessary to accomplish the desired match between the phase P* and the unit's and ten's of the Line Number Register. A reduction in the number of first levels has been obtained by making use of both primed and unprimed outputs of the line number ten's trigger pairs.

The time lapse between the occurrence of a match and the operation of the code corresponding to the given line number is four number times. The total delay involved in a matching operation will be increased if the

unit's number time match does not occur at once. The phase match depends not only on the phase of the drum, P, but also on the pole piece selected by the trigger pairs PP. By selecting the proper set of pole pieces a phase match may be obtained at any point along the circumference of the drum. The selection of this set is controlled by the matching circuit and the Main Control Ring (MCR). Figure 4-26 shows as an example the circuit for pole piece selection trigger pair PP2'. Level 1 of this circuit is the hold level which keeps the trigger pair in its low state from 3-8 digit times and from 10-1 digit times. In addition level 2 will hold the circuit as long as the output MCR3 is low. Level 2 will be low during regular running operation, and high while the circuit is waiting for a match. While the machine is trying for a match, the outputs MCR4', 3' and 2 are low so that level 3 of this circuit will be low at 8 digit time. When the output of PP2' is low, all other outputs PP' are high, and one of five outputs P*' will be low corresponding to the phase of the machine at that moment. This output P*' is fed directly into the matching circuit. In case a match is obtained, the output of M-3 will be low and will step the Main Control Ring. In case no match is obtained the Main Control Ring will remain unchanged. At 9 digit time level 3 is no longer low and level 1, "Hold 1," is high, preventing the trigger pair from locking itself in. At that time a similar operation is performed in PP3' which therefore is low at 9 digit time and again will be opened up at 10 digit time. It is possible that the trigger pair PP2' may have been selected in a previous reading operation and consequently would still have been low at the moment of the first try. In order to avoid this situation, which might lead to ambiguity, the pole piece selection trigger pairs are all reset at 2 digit time on hold level 1, when MCR3 is high. When a match succeeds, the

ring will step so that MCR3 becomes low and MCR3' high. For PP2 this will happen during 8 digit time. As a result level 3 is no longer low since the condition (MCR4')(3')(2)(8 DT') is no longer satisfied. However, the output of this trigger pair is still low since the circuit holds on hold level 1 in which both PP2' and the inputs 2DT and 9DT are low. Since during this digit time the output MCR3 has become low, the circuit will now hold on level 2 where both PP2' and MCR3 are low. As a result of the change of state of the Main Control Ring, none of the other pole pieces will be pulled low after this moment. Thus the desired set of pole pieces is selected by trying in succession each of the five sets in consecutive cycles.

In recording operation the match corresponding to pole piece set 0 should be obtained, because the record relays must be connected to the pole pieces at position I (Fig. 4-21), corresponding to PP0. It is necessary therefore that no other pole piece produce a match in the M-3 circuit. The relay control input K1-6' therefore makes the -45 V supply terminal in each of the circuits PP1'-PP4' high, thus preventing any one of these trigger pairs from producing a match in the matching circuit. During the digit time in which a match succeeds, several operations have to be performed in succession. Assume that each of these operations would take 10 microseconds, which is several times the observed speed of the circuit. Then 10 microseconds after the beginning of the digit time the output of PP2' would be low, 20 microseconds afterwards P*2' would be low, 30 microseconds afterwards M-3 would be low, and 40 microseconds afterwards PP2' would hold. With a digit time of 60 microseconds this is in time to preserve the state which has been selected.

E. First Sequence Trigger Pairs

The purpose of the First Sequence Trigger Pairs (FSTP) is to store the twenty code digits of the sequence code. These twenty digits can be read in from the drum, from the sequence tape, or from manual control. From the First Sequence Trigger Pairs the code digits can be read out to the Second Sequence Trigger Pairs, to the record unit, to the External Transfer Register, or to the indicators. The First Sequence Trigger Pairs allow the code to be changed subject to several controls such as the I, J, K and Conditional Call controls. The outputs of the First Sequence Trigger Pairs control the wait circuit, as is described in Part J.

Figure 4-27 shows the First Sequence Trigger Pairs in the lower part of the drawing. Auxiliary controls are indicated in the upper part of the drawing. The sequence code consists of three main parts: the α code, the β code and the γ code. The α code consists of four binary code digits, called sequence code digits 1-4. Sequence code digit 1 is also called the α ten's digit, while code digits 2, 3 and 4 form the α unit's digits. These second names refer to the decimal representation of the sequence codes. Whereas the sequence code appears in its 20-digit binary form in the First Sequence Trigger Pairs, its eight decimal digit form appears in the indicators, or on the Fast In-Bus, as read out from the sequence tape, or from manual control. The α codes are labelled by the numbers 00-07 and 10-17. The digit in the ten's place of this number corresponds to the state of first sequence trigger pair 1' as indicated in Fig. 4-28. A decimal 0 corresponds to a binary 1, indicating that the primed output of the trigger pair is low. The eight output states of trigger pairs 2', 3' and 4' correspond to the decimal numbers 0-7, as indicated in Fig. 4-28. The β part of the code corresponds to the

first sequence trigger pairs 5' to 14'. 5' and 6' are called β hundred's, 7', 8', 9' and 10', β ten's, and 11', 12', 13' and 14', β unit's. The four states of the β hundred's and their decimal equivalents again are indicated in Fig. 4-28. The β ten's and β unit's set of trigger pairs each have sixteen states. A set of ten of these states corresponds to the decimal digits 0-9. The remaining set of six states, marked 10-15, will also appear in the ten's or unit's column as 0-5. To determine whether a digit in the range 0-5 belongs to the first or second of these sets, a fourth decimal digit, the β thousand's digit, is introduced. This thousand's digit appears only in the decimal form of the codes. Figure 4-28 shows the relation between the thousand's digits and the group to which the β unit's and β ten's digits belong. The γ digits include code digits 15, 16 and 17 which form the γ ten's digits, and code digits 18, 19 and 20 which are the γ unit's digits. Their number system corresponds to that of the α unit's.

Reading in from the drum is controlled by the output DRUM' of the sequence playback, shown in Fig. 4-9, and occurs at the digit times which are shown in Fig. 4-16. It is not possible to read code digits 1-5 directly to first sequence trigger pairs 1'-5'. Instead, they are read into the trigger pairs marked ICTR, JCTR, KCTR, LCTR and MCTR (Fig. 4-27). These are intermediate storage trigger pairs, all of which have other functions as well. The first five code digits are read in here at 18,..., 2 digit times, respectively, and are simultaneously advanced to first sequence trigger pairs 1'-5' at 3 digit time. All the First Sequence Trigger Pairs are reset at 2 digit time preceding the read-in from the auxiliary trigger pairs or from the DRUM' signal. The reset is controlled by the selenium circuit marked FSR, Fig. 4-34, and has a low output at 2 digit time which,

after inversion, gives a high unprimed FSR to the hold level of all the First Sequence Trigger Pairs. At 3 digit time code digit 6 is read into first sequence trigger pair 6', at 4 digit time sequence code digit 7 is read into first sequence trigger pair 7', and so on, until code digit 20 is read to first sequence trigger pair 20' at 17 digit time.

A second mode of read-in to the First Sequence Trigger Pairs is from the Fast In-Bus (FIB). This mode occurs in manual read-in of codes, where the code appears on the bus and is read into the First Sequence Trigger Pairs. It also occurs in the part of the recording operation in which the code is read from the tape mechanism onto the bus and, following translation into its binary form, into the First Sequence Trigger Pairs, from which it is later read to the drum. A code is recorded in columns 1-8 of the sequence tape as a decimal number, with the γ units digit in the unit's column, γ ten's digit in the ten's column, and so on, with finally the α-ten's in the column for 10^7. The code is read by the tape mechanism from the tape to the Read Register, and subsequently read out to the Fast In-Bus. The unit's, or 10^0, digit of a number that is transferred, appears at 2 digit time on the Fast In-Bus. Hence, the γ unit's digit appears at the Fast In-Bus at 2 digit time, the γ ten's at 3 digit time, and so on, to the α ten's which appears at 9 digit time at the Fast In-Bus. Each of these digits is read to the First Sequence Trigger Pairs with a transformation such that the number appears in its binary form. The β thousand's digit is not read into the First Sequence Trigger Pairs but into the trigger pairs LCTR and MCTR. It is stored in the number system shown in Fig. 4-28. With the code read in in this fashion, the α and γ codes as well as the β hundred's are stored in their correct binary configuration. As far as the β ten's and β unit's are concerned, the decimal

digit is read into the trigger pairs 7'-10' and 11'-14', respectively, without any translation. This assumes that the digits belong to the first set. If the decimal digit read in belongs to the first group the trigger pairs will remain unchanged. If, however, the decimal digit belongs to the second group (the digit 10-15), it has to be changed to its proper binary equivalent. This change is controlled by the outputs of the trigger pair LCTR' for the β ten's and MCTR' for the β unit's. The β thousand's code digits are read into the LCTR' and MCTR' trigger pairs at 7 digit time. During 8-11 digit time the outputs of these trigger pairs control a change in the binary configuration of the β ten's and β unit's digits. These changes are shown in Fig. 4-29 for all the decimal digits 0-5 which are changed from their binary equivalent to the binary equivalent of the numbers 10-15. Figures 4-30 - 4-33 show as an example the logical conditions for the trigger pairs FSTP11'-FSTP14'. The read-in operation is controlled by the circuit FSRI, Fig. 4-34, which operates both when reading in from the sequence tape and in manual control read-in. The circuit FSRI in turn controls the circuit FSR which resets the First Sequence Trigger Pairs at 0 digit time in case of a read-in from the bus. In the case of recording, when a number is transferred from the sequence tape to the First Sequence Trigger Pairs and then onto the drum, the entire code appears on the bus in the course of one number time. This is in contrast to the case of manual read-in when only one digit at a time appears on the bus as the digits are read in manually. Manual read-in requires special controls to take care of the β thousand's transformation, which will be discussed in Part L.

During the time the code is read in from the drum into the First Sequence Trigger Pairs, the IJK controls and the Conditional Call control

can take place. For the I control the code digits 5-10 are replaced by the number available in the I Register. For the J control, the code digits 11-14 are replaced by the number in the J Register. For the K control, the code digits 5-14 are altered according to the number which is stored in the K Register. The I, J and K Registers, together with the Condition Register, are shown in Fig. 4-35. The read-in, reset, and read-out of these registers will be discussed in Part G. The numbers are stored in the I, J and K Registers in such a way that they can be read in without translation to the First Sequence Trigger Pairs.

The change of the sequence code digits 5-14 in case of an I, J or K control occurs under control of the trigger pairs ICTR, JCTR and KCTR (Figs. 4-36 - 4-38). These trigger pairs are reset at 11 digit time, and tripped at 12 digit time under control of the code digits 5-10 and 11-14 or 5-14 respectively. An auxiliary reset IJKR (Fig. 4-39) can occur at 13 digit time, and is used to simplify the conditions for which I, J or K control occurs. In case one or more of the I, J or K Registers are not reset, they control at 14 digit time the reset of the First Sequence Trigger Pairs involved in the I, J or K control, and subsequently at 15 digit time allow the read-in from the I, J and K Registers to the First Sequence Trigger Pairs. The codes indicating an I control have the code 1111 in the β ten's column, although not all codes containing this combination have I control. The ICTR circuit produces a low output when First Sequence Trigger Pairs 6, 7, 8, 9 and 10 have their primed outputs low, as is shown in Fig. 4-36. This takes care of all the desired I codes. It also incorporates the codes 3002, 3003, and 3200 which are not I codes, and a number of codes which have not yet been assigned. These undesired codes, however, respectively make levels 1, 2 and 4 of the circuit IJKR

low, as shown in Fig. 4-39. The output of this circuit is combined in a T_2 with 13 DT' furnishing the reset IJKR for the circuits ICTR, JCTR and KCTR. Figures 4-37 and 4-38 show the logical specifications of the circuits JCTR and KCTR, together with the circuit IJKR, which provide the conditions for J and K control. The relay control of the -45 V supply terminal for the circuits ICTR, JCTR and KCTR prevents the I, J or K control from taking place when the machine is stopped, in case of a reading operation, and in case of a record operation.

In addition to the I, J and K controls, the code standing in the First Sequence Trigger Pairs is altered when a conditional call code occurs. If the conditional call is met, the conditional call code is changed to a call code. If the conditional call code is not met, the code remains unchanged. There is no final code that corresponds to the conditional call code. Thus if the conditional call is not met, even though the code is advanced, no operation is performed. The code, "to call register and call," is the β code 11 0111 1111. The code, "to call register and conditional call," is 11 0111 0111. The codes differ in sequence code digit 11. If the conditional call is met, the state of FSTP 11' is changed so that its primed output is no longer high but low. Figure 4-30 shows the conditions for FSTP11'. Level 6, in conjunction with the associated card FSTP11'A, takes care of the conditional call code. It includes all the code digits 5-14 with the exception of 11 itself and the timing pulse 17 DT'.

The code in the First Sequence Trigger Pairs is advanced during 18 digit time into the Second Sequence Trigger Pairs. The advancing operation will be discussed in Part G, which describes the Second Sequence Trigger Pairs. Figure 4-9 shows the output of the First Sequence Trigger

Pairs to the record unit. The First Sequence Trigger Pair outputs are combined with 0-19 DT, in the circuit REC, as described in Part D. The First Sequence Trigger Pairs also have an output to the circuit LNCO (Fig. 4-40). The outputs of the First Sequence Trigger Pairs and the Line Number Register are fed to the indicator circuit as will be described in Part K.

The code digits 5-20 may represent a 4-digit decimal number to be read into the γ Transfer Register through the external transfer circuits. The outputs of the First Sequence Trigger Pairs to the γ Transfer Register are discussed in Part H.

F. Special Registers

The following special registers are included in the sequence circuits: a) I-J Register, b) K Register, c) Condition Register, d) Call Register. The I-J Register (Fig. 4-35) is a trigger pair register capable of storing the numbers 000-399. The hundred's and ten's digits are stored in the I Register; the unit's digit is stored in the J Register. The J Register has a read-in or read-out under control of the code β3002; the I-J Register has a read-in or read-out under control of code β3003. The I Register has no separate read-in or read-out. However, either the I or the J Register, or both simultaneously, may be used to control the code, as is explained in the description of the First Sequence Trigger Pairs. Figure 4-41 shows, as an example, the logical specifications of J8, I-20, I-100 and I-200. Level 1 of J8 is the hold level which permits the trigger pair to be reset under control of the output, "J Reset." This output is derived as shown in Fig. 4-35 from a combination of 1 DT' and the output of J Read-In (JRI). JRI is shown in Fig. 4-42. Level 1 will be low when code β3002 occurs simultaneously with the input β out, signifying a read-in to the J Register. Level 2 is low when the code β3003 occurs together with β out, for a read-in to the I-J Register. The output of JRI feeds level 2 of J8, permitting a read-in at 2 digit time from the 8-wire of the Fast In-Bus. The output JRI also feeds the read-in level of the I Register as shown in the specifications for I-20, level 2. Since a read-in is desired only for the code β3003 and not for the code β3002, the input βU13' has been added to this level. The circuits of I-100 and I-200 operate in similar fashion, except for the translation which has to be made on reading in.

The K Register consists of five trigger pairs (Fig. 4-35). Its operation is similar to that of the J Register. The logical description of the Condition Register is given in Fig. 4-44. During the read-in operation a sign is read from the bus into the Condition Register under control of code β3012. The necessary reset is performed in level 2 of circuit CC; the read-in occurs under control of the joined levels of circuit CC'A. The output of the Condition Register is used in FSTP11' at 17 digit time as mentioned in Part E.

The read-out to the Regeneration Circuit from the I, J, K and Condition Registers is accomplished by the circuits IJKO-8, IJKO-4, IJKO-2, IJKO-1 and IJKRO. The latter circuit is shown in Fig. 4-43. The four levels of this circuit correspond to read-out codes for the K, J, IJ and Condition Registers, respectively. If any of these four codes occurs, the output of the circuit will be low. Figure 4-45 shows the circuit for IJKO-8. The inputs to each level in these circuits include the output of the desired trigger pair, the proper digit time and the signal IJKRO'. In order to distinguish among the four possible codes, one β code digit has been added to each level. For example, the read-out from the J Register can happen for two codes, β3002 and β3003. Both have the same β ten's digit, βT10'. This is included on level 2 of the read-out circuit IJKO-8. Since reading out from the J Register should happen only under control of code β3003, the β unit's digit βU13' is used on levels 3 and 4. The outputs of these selenium circuits are inverted and fed into cathode followers as shown in Fig. 4-35. Each of the cathode followers shown in Fig. 4-35 is a section of the C_4 shown at the corresponding terminals in Fig. 4-46. The four sections are connected to a common cathode resistor, and are fed by the IJKO circuits, the Line Number

Register, the Slow Storage Control Register, and the Manual Control Circuits, respectively. Figure 4-46 shows how the digits read in to the Regeneration Circuit are advanced and read into the Fast In-Bus trigger pairs FIB8, 4, 2 and 1.

Whenever a call code (β3010) is given, the line number of the next line of coding to be performed is read from the Fast In-Bus to the Line Number Register. In addition this line number is read to the Call Register. The number read into the Line Number Register is destroyed during the call operation. However, it will remain in the Call Register until another call operation is performed. Thus, unless further read-ins to this register are coded, the Call Register will retain the number of the last line called. This is useful in checking operations, to show the point at which the last sequence of codes began.

The Call Register is a magnetic delay line shown in Fig. 4-40. The input windings of the delay line are in common with those of the Fast Storage Registers 40-79. The outputs of the delay line feed the Regeneration Circuit. The delay line is advanced under control of the circuit CRA, shown in Fig. 4-47. Level 1 is low under control of the call code (β3010) and level 2 is low for the code β3013, "Call Register in" or "Call Register out."

G. Second Sequence Trigger Pairs

The First Sequence Trigger Pairs act on code numbers, and may modify them under instructions such as the I-J control, but they do not directly control the operations of the machine. Such control is the function of the Second Sequence Trigger Pairs. These are selenium circuit trigger pairs which are set under control of the First Sequence Trigger Pairs during 18 digit time and which are reset by SSTPR (Fig. 4.49) during 18 digit time.

In this way the outputs of the Second Sequence Trigger Pairs corresponding to the code stored in the First Sequence Trigger Pairs will be low shortly after the beginning of 18 digit time. The outputs will remain low until 18 digit time of the next cycle. At that time the trigger pairs will either be reset or remain low depending on the next code. Figure 4-48 shows that for each of the Second Sequence Trigger Pairs level 1 will be high under control of SSTPR. At the same time level 2 will be low for those selected under control of the First Sequence Trigger Pairs and the code advance signal CA (Fig. 4-50). The Second Sequence Trigger Pairs consist of three groups corresponding to the three parts of the sequence code, the α, the β, and the γ trigger pairs. The read-in from the First Sequence Trigger Pairs to the β and the γ Second Sequence Trigger Pairs is made with a translation. This translation is indicated in Fig. 4-50 and Fig. 4-51 and in the examples of Fig. 4-48.

A code standing in the Second Sequence Trigger Pairs is identified by the low outputs of three β trigger pairs and two γ trigger pairs.

The circuits controlling the code advance (CA) are shown in Fig. 4-49. When the machine is running, the second level of the circuit CA operates during 18 digit time. The operation is controlled by the Main

Control Ring which will be described in Part J. The first and third levels take care of two manual controls, the Operate and the Repeat button. The advancing of the β part or the γ part of the code can be prevented by the circuits βCAR and γCAR (Fig. 4-49). This is the case for an external transfer code, when the advancing of the β and γ part of the code is prevented under control of the signal XT'. A second case occurs in reading numbers to the indicators. Only the part of the code which controls a read-out is advanced. This is the α code together with either the β or the γ part of the code. The levels of βCAR and γCAR controlled by the relay contact C1-3 prevent the advancing of the unwanted part of the code.

H. External Transfer and γ Transfer Circuit

The γ Transfer Register functions as an intermediate storage register in the transfer of numbers from a register on the β side of the machine to another register on that side. Such a transfer must be performed in two steps: first, reading out the number from the β register to the γ Transfer Register, and second, reading from the γ Transfer Register to another β register. The γ Transfer Register is also used in the external transfer operation, when the sequence code digits 5-20 are read, under control of an α code, through the External Transfer Register into the γ Transfer Register. The sixteen code digits 5-20 are so regrouped as to form four decimal digits. Two kinds of external transfer are possible. In the first kind, external transfer with reset, the four decimal digits are placed in columns 1-4 of the γ Transfer Register and columns 5-16 are reset to 0. In the second kind, external transfer with shift, the four decimal digits are placed in the columns 1-4, while the digits which were available in columns 1-12 of the γ Transfer Register are shifted four columns, to columns 5-16, respectively. The digits formerly in columns 13-16 of the γ Transfer Register are destroyed in the course of this operation.

The circuits controlling the γ Transfer Register and the external transfer operation are shown in Fig. 4-52. They control four operations: a) read-in to γ Transfer Register under control of the γ code 00 and an α code indicating a transfer from the β side to the γ side; b) read-out of γ Transfer Register under control of γ code 00 and an α code indicating a transfer from the γ side to the β side; c) external transfer with reset, under control of α code 04; and d) external transfer with shift, under control of α code 05. In order to perform these different

operations, use is made of two delay lines, the γ Transfer Register, and the External Transfer Register. Cores 16-1, on each of the 8, 4, 2 and 1 lines of the γ Transfer Register, are advanced by D_1 and D_2 pulses under control of the selenium circuit γTRA (Fig. 4-53). The first D_1 core on each line, marked 17, is controlled by a D_1 pulse gated by the selenium circuit γTRL1. The last cores of the 8, 4, 2 and 1 lines of the γ Transfer Register are similarly controlled by a D_2 pulse gated by the circuit γTRL2. The pulse windings of the D_2 cores 0 feed directly into the D_1 cores 17. These connections are indicated by the letters t, u, v and z. In addition, the γ Transfer Register has a read-in in the D_1 cores marked 17 and a read-out from the D_2 cores 0. The last cores of the External Transfer Register are advanced by D_2 pulses controlled by the output XTC'. From these cores, information is advanced into the D_1 cores 16 of the γ Transfer Register via the connections indicated by the letters p, q, r and s. The read-in to the External Transfer Register occurs under control of the circuits XTO-8 - XTO-1 (Fig. 4-54). The circuits for the advancing of the External Transfer and γ Transfer delay lines and the linking cores are shown in Fig. 4-53. A pulse diagram for the four operations associated with the γ Transfer Register and the External Transfer Register is shown in Fig. 4-55.

During the operation "γ Transfer Register In," the number to be read from the β side of the machine into the γ Transfer Register will appear from 0-16 digit time at the Fast Out-Bus (FOB). The read-in is performed by advance pulses gated by γTRA and γTRL1 occurring during 0-17 digit times as shown in Fig. 4-55.

In reading out of the γ Transfer Register the outputs of γTRA, γTRL1 and γTRL2 are low. During 0-17 digit times all cores of the γ Transfer

Register are advanced, and since D_2 core 0 feeds into D_1 core 17, the information held in the delay line will be regenerated. Since eighteen cores are used and eighteen advancing pulses supplied, the information is returned to its original position. At the same time the number is read from the delay line to the Regeneration Circuit (Fig. 4-46).

The external transfer operation takes place in two successive machine cycles. In the cycle during which the external transfer code is operating, and the cycle immediately preceding it, the code digits 5-20 as stored in the First Sequence Trigger Pairs are read through the circuits XTO-8 - XTO-1 into the External Transfer Register. This register is advanced during 17 to 1 digit times by the circuit XTRA. During this time either code "External Transfer with reset" or code "External Transfer with shift" is standing in FSTP1' - FSTP4' and controls the output XT' (Fig. 4-53). This output, in turn, makes level 1 of the circuit XTRA low from 17 to 1 digit times. The unit's digit of the number being transferred is formed by the four code digits 6, 18, 19, 20; the ten's digit by the code digits 5, 15, 16, 17; the hundred's digit by the code digits 11, 12, 13, 14; the thousand's digit by the code digits 7, 8, 9 and 10. In the external transfer operation with reset, the circuits γTRA, XTRA and XTC' are low as shown in Fig. 4-53. The cores of the γ Transfer Register are advanced during 17 to 1 digit times under control of XT', and from 2 to 17 digit times, under control of XTC'. Thus the External Transfer Register is advanced by 21 sets of pulses from 17 digit time of one cycle to 17 digit time of the following cycle (Fig. 4-55c, lines 6 and 7). The unit's digit of the number to be transferred is read in to the External Transfer Register at 18 digit time. It is advanced through the External Transfer Register and read into D_1 cores 16 of the

γ Transfer Register at 2 digit time. The unit's digit is further advanced through 17 digit time, when it is read into cores 1. The ten's, hundred's, and thousand's digits follow the unit's digit and are stored in γ Transfer Register cores 2, 3 and 4.

During this type of external transfer no information appears on the Fast In-Bus. Figure 4-54 shows that on level 5 of XTO-8 the signals (binary zeros) on the Fast In-Bus are read in from 2 to 16 digit times into the External Transfer Register. Hence, in external transfer with reset, no pulses will be introduced into the 8-line of the External Transfer Register; the same is true of the 2-line. For the 4-line and the 1-line a binary 1 is generated from 2-16 digit times (Fig. 4-54). In this manner, coded decimal zeros are formed and read into the External Transfer Register. They immediately follow the digits of the number externally transferred, and finally appear in the cores 5-16 of the γ Transfer Register, thus completing the operation of external transfer with reset.

The operations for the external transfer with shift are identical to those for the external transfer with reset during the cycle preceding the presence of the external transfer code in the Second Sequence Trigger Pairs. During the cycle in which the external transfer code is operating, the advancing circuits XTRA, γTRA, and XTC' are used again. In addition, the circuit γTRL2 has a low output. The number previously held in the γ Transfer Register is read out to the Regeneration Circuit (Fig. 4-46) during this cycle. The information available at the output of the Fast In-Bus trigger pairs may now be read in to the External Transfer Register during 2-16 digit time by means of the circuits XTO-8 - XTO-1. In this way the unit's digit of the number previously stored follows the thousand's digit of the number transferred from the First Sequence Trigger Pairs.

The information previously in the cores 1-12 will be placed in cores 5-16 of the γ Transfer Register.

The code digits 5-20 which are used in the external transfer operation normally form the β and γ parts of the code. To avoid spurious use of these code digits as β and γ codes, they are prevented from advancing into the β and γ Second Sequence Trigger Pairs under control of the signal XT', as shown in Fig. 4-49. The code digits 5-20, while standing in the First Sequence Trigger Pairs, may ordinarily be used in the wait operation and for the I, J, K and conditional call control. When external transfer occurs, the wait operation is prevented by the output XT, as shown in Fig. 4-9 (Part J). Again in the case of external transfer, the digits stored in the first sequence trigger pairs 7-10 and 11-14 correspond to the β codes βT0 - βT9 and βU0 - βU9, respectively. As neither the I, J, K nor conditional call controls make use of these β code digits, there will be no interference with the external transfer operation.

J. Main Control Ring

The Main Control Ring is used 1) to provide the internal cycling required by the operations Call, Wait and Stop; 2) to provide connections between the switches of the control panel with their associated relays, and the electronic cycling of the machine; 3) to provide the pulses necessary to operate the step switches and some of the relays associated with the control panel. The construction of the Main Control Ring is shown schematically in Fig. 4-56. It consists of the four trigger pairs MCR4, MCR3, MCR2 and MCR1. In the Main Control Ring seven cycles are used, and each will be discussed in turn. The cycles are indicated schematically in Fig. 4-57, columns 1-7. At the left of this figure, under the heading "Main Control Ring," the outputs of the four trigger pairs involved are designated by the numbers 4, 3, 2 and 1. With four outputs, sixteen possible states are available, marked 1-16 in this column. A one indicates that the unprimed output is high and the primed output is low. In columns 1-7 the different orders in which the outputs of the trigger pairs may be cycled through their sixteen states are indicated. The seven cycles are the following: 1) Call; 2) Wait; 3) Stop; 4) Step Switch; 5) Next Line; 6) Specified Line; and 7) Record. In addition, columns 8-25 show some of the operations which are performed during the steps of the Main Control Ring. The operations are indicated on the same horizontal line as the corresponding output of the Main Control Ring. The output configurations of the trigger pairs MCR4, MCR3, MCR2, MCR1 required to control these operations are indicated by the symbols 0, 1 or X. An "X" indicates that the corresponding output is not sensed. When only the MCR output conditions are considered, some operations can be performed in several states of the Main Control Ring. However, the operations are listed only

for those states where auxiliary conditions are such that they actually will be performed. The sheets indicating the logical conditions for the trigger pairs MCR4, MCR3, MCR2 and MCR1 are shown in Figs. 4-58 - 4-61. Closely connected with the Main Control Ring is the Stop trigger pair (Fig. 4-56) with outputs S and S', whose logical conditions are shown in Fig. 4-62 and the circuit GO' whose specifications are given in Fig. 4-64.

Call Cycle

This cycle is used whenever the call code β3010 (in) appears in the Second Sequence Trigger Pairs while the machine is running. This occurs when a call code is read from the First Sequence Trigger Pairs, or when a conditional call code, β3011, is modified in the First Sequence Trigger Pairs under control of the Condition Register. Under control of this code the following operations are performed: a) the cycling of the Line Number Register is stopped, b) the reading and advancing of codes is stopped, c) the number of the line to be called is read into the Line Number Register, d) a match is obtained between the number in the Line Number Register and timing pulses of the drum, and the desired pole piece is selected, e) the cycling of the Line Number Register is resumed, f) the reading and advancing of codes is resumed. The timing of these operations is controlled by the Call Cycle.

While the machine is running the Main Control Ring stands in position 1, the outputs of all four trigger pairs being 0. In addition, the output S of the Stop trigger pair is low. This trigger pair in turn controls the relay J1, which is picked up when S is low. The relay J1 has two sets of contacts. Contact J1-2 is used to connect the -45 V supply terminals of various trigger pairs to -45 V. Without this connection the

terminals are connected to ground through a 10K resistor. Contact J1-1 is used to control the Stop and Go lights, shown in Fig. 4-56. The output S is low when the machine is running or engaged in a recording operation. In the latter case, as is shown in Part L, either relay K1 or relay K3 will be picked up. The output K3-6' will be connected to -45 V when the machine is in operation and not recording. The output J1-2' will be connected to -45 V when the machine is stopped. Level 3 of MCR1', Fig. 4-61, shows that during 1 digit time of the cycle in which the β3010 in-code appears, the output MCR1' will be made low. This is done by the output LNRRI' which will be low, and by the output βT11', which is used to distinguish this code from the others which can make LNRRI' low. Because of this change the ring steps to state 2. In Fig. 4-59 level 4 of MCR3' shows that as the ring reaches state 2, the output 3' will become low at 2 digit time and the ring will step to the state identified by the outputs 0101, which is state 5. As indicated in Fig. 4-57, column 1, the ring now steps from state 5 to state 8 during 5 digit time since the output MCR4' becomes low. This is shown by the conditions for level 3 of MCR4', Fig. 4-58. When the output MCR3' becomes low during 2 digit time, the output MCR3 becomes high and the trigger pairs PP0' - PP4' will be reset. This is described in greater detail in Part D. After the ring reaches state 8 at 5 digit time, the level marked "Try" in the pole piece selection trigger pairs (Fig. 4-26) will become low during the appropriate digit times. This will allow a match, m-3 and M-3, to occur when the proper number time and phase are present. When the outputs of the circuits m-3 and M-3 become low, level 5 of the circuit MCR3 also becomes low and the ring steps to state 9. This allows the desired pole piece selection circuit to lock in, and completes that part of the Call Cycle which is concerned with the selection

of the set of pole pieces from which the codes are to be read. Once the match has occurred the Call Cycle provides the necessary time delay between this moment and the moment at which the codes should be available in the First Sequence Trigger Pairs. The match occurs four number times before the moment M in which the code is to operate, as mentioned in Part D. The match may occur in any of the digit times 6-10 of number time M-4 and the ring will step during 14 digit time of that number time from state 9 to state 10; during number time M-3 it steps to state 15; during M-2 it steps to state 14, and during 8 digit time of M-1 to state 1, which is the normal operating state of the ring. During the last two steps of the cycle, the signal GO' (Fig. 4-64; column 14, Fig. 4-57) has been low, allowing first a reset, then a read-in from the drum into the First Sequence Trigger Pairs and from the signals P*, NT, and E2 to the Line Number Register. This part of the operation is not in common with the Record Cycle, hence is controlled by the output K3-6'. In this way code digits are read into the First Sequence Trigger Pairs beginning at 10 digit time of number time M-2. The code is advanced from the First Sequence Trigger Pairs to the Second Sequence Trigger Pairs under control of the circuit CA (Fig. 4-49). Level 2 of this circuit shows that the code advance occurs during 18 digit time when both GO' and MCR2 are low. This is the case only for state 1 of the Main Control Ring. The code advance therefore is resumed during 18 digit time of the cycle M.

Wait Cycle

Several operations of Mark IV require more than one number time. In some cases, such as multiplication, the length of the operation is known in advance, but in other cases it is not. In the slow-fast or fast-slow

storage transfer, the amount of time necessary depends on the position of the drum with respect to the reading or recording pole pieces. In the case of the tape read or record operation, the time required depends on the location of the information on the tape. Whenever an operation occurs which takes more than one number time, precautions must be taken to insure that a conflicting operation is not started before the preceding one is finished. In the case of the multiplier, the timing is controlled by the coding. In the case of slow-fast or fast-slow transfer, or in the case of recording or reading from tape, a Wait circuit is used. The main part of the Wait circuit consists of a selenium card which combines the information obtained from the units engaged in an operation with the code digits as stored in the First Sequence Trigger Pairs.

The Wait circuit is shown in the schematic diagram, Fig. 4-9. The output of the selenium card is combined in a T_2 with the output XT, amplified and sent to the selenium card for MCR1'. The input XT will be high when an external transfer code is standing in the First Sequence Trigger Pairs. The inputs to the Wait circuit belong to the α and β sections of the code as read into the First Sequence Trigger Pairs or, possibly, as changed at 15 digit time under the I, J or K control. At 17 digit time the output of the Wait circuit is used to make low the output MCR1' thus stepping the Main Control Ring from state 1 to state 2. This is done under control of the -45 V supply through relay K3-6', eliminating those occasions during which the machine is either stopped or engaged in a recording operation. Stepping to state 2 during 17 digit time makes the signal GO' high, and eliminates the code advance signal (CA) which occurs during 18 digit time as shown in column 15. During 2 digit time following the Wait signal, the ring is placed under control of the Call Cycle, then

steps to state 5 and continues the Call Cycle described earlier. The ring leaves its home position during 17 digit time just after the line number of the next code to be performed, that is, the code causing the Wait, has been read into the Line Number Register. During the Call Cycle the match is performed with this number still in the Line Number Register. A total of five number times is used in a Wait operation. As far as the pole piece selection is concerned, this amounts to selecting the pole piece ahead of the one which was operating when the Wait command occurred. During number time M-1 the desired code again is read to the First Sequence Trigger Pairs. If the Wait condition still prevails, another Wait will be introduced; if not, the regular reading of commands begins on the next cycle.

Stop Cycle

Figure 4-62 shows the logical specifications for the Stop trigger pairs S and S', and indicates the different conditions under which the machine can be stopped when running. While the machine is running the output S will be low and S', high, and conversely when the machine is stopped. A stop can occur under control of two β codes, β1312, "Stop," and β1313, "Check." The machine will stop when a number is transferred over the Fast In-Bus with a negative sign while either of these two codes is operating. Levels 6 and 7 of S' are used for these two codes, respectively. The sign appears on the Fast In-Bus during 1 digit time. A positive sign is represented by the code 0000, and a negative sign by 1000. Hence, when the sign is negative, FIB8' is low making the output of S' low, and stopping the machine.

A second mode of stopping the machine is manual control. As mentioned in Part B, the machine may be stopped either instantaneously

under control of the Stop button, or at the line indicated by the Stop Line Number strip switch under control of the Stop toggle switch. The Stop button is an emergency stop capable of stopping the machine while it is running and the Main Control Ring is standing in state 1, or, for some reason, stuck on step 7 or step 8. One reason why the Main Control Ring may get stuck on step 7 or step 8 is that the number read into the Line Number Register may contain improper binary digits such that no match with the phase or number time can be obtained. For all other states, the Main Control Ring will continue to step under control of digit time, number time or phase pulses applied continuously from the basic timing rings. With both the Main Control Ring and the timing rings operating properly, the ring can not get stuck in any position other than the states 1, 7 or 8. The Stop button has been designed to operate on specified states of the Main Control Ring in order to prevent a stop from occurring during a normal Call or Wait cycle. As the Stop button is pushed, the relay J2 is picked up as shown in Fig. 4-56 and will remain picked up until the Stop operation has been completed. The relay J2, through its contact J2-3, applies -45 V to levels 9 and 10 of the selenium circuit for S'.

Level 5 of the circuit for S' becomes low during 0 digit time when a Stop match occurs. This is the case when the number in the Line Number Register is identical to the number in the Stop Line Number strip switches, and the Stop Specified Line toggle switch has been thrown. The circuit SM, shown schematically in Fig. 4-56, is discussed in Part L. When a Stop match occurs, the output of the selenium circuit SM goes high, and when inverted, gives a low input SM to the circuit S'.

In the description of the Record Cycle it is shown that a line

number and code are read in succession from the sequence tape. When a code is read instead of a line number or vice versa, a stop must be introduced to show that a line number has been read into the First Sequence Trigger Pairs or a code into the Line Number Register. This stop is introduced in levels 2 and 3 of the circuits S'. Level 4 of the circuit of S' is low during the operation under control of the One Line button, as described in greater detail in Part L.

In the Main Control Ring and the Stop Trigger Pairs each trigger pair consists of several selenium cards. In the case of the Stop Trigger Pairs the 12 levels for S' are located in five selenium cards marked S', S'A, S'B, S'C and S'D. This kind of construction is used to allow both greater uniformity of the components employed in the whole sequence mechanism and greater flexibility in servicing and alterations. In case of the Stop Trigger Pair, other conditions for which it may be desired to have a Stop, such as an alarm, may be introduced by adding more selenium cards to the present circuit. The Stop Trigger Pair is reset in the levels of the circuit S, under control of the Start, One Line, and Record buttons.

Stops occur during 0 digit time or 1 digit time and cause the Main Control Ring to step from step 1 to step 7 during 1 digit time. If the ring is already standing on step 7, or standing on step 8, it will remain there until relay J1 has dropped out. The control ring can no longer step under control of the Call Cycle or the Next Line Cycle, as both the step from 7 to 16 and the step from 8 to 9 require that the output S be low. When, however, the relay J1 has dropped out, the Step Switch Cycle discussed below becomes operative. It should be noted that the step from 1 to 7 under control of the low output S' can occur only at a moment when the relay J1 is not yet dropped out and its contact J1-2 is still

providing -45 V to level 6 of MCR3' and level 5 of MCR4'. When the machine is stopped and no manual operations are performed, the Main Control Ring is in state 1 and the Stop trigger pair has its output S' low. In this case the ring cannot move from state 1 to state 7 since the relay J1 is not picked up.

Step Switch Cycle

The purpose of the Step Switch Cycle shown in Column 4 of Fig. 4-57 is to control the four step switches used in the sequence mechanism. Both the pulses required for the step switches and the control for the beginning and the end of the Step Switch Cycle are provided by the Main Control Ring. Only the electronic cycling part of the operation will be discussed here. When the Main Control Ring is standing in state 7 with the J1 relay dropped out, it will advance to step 8 under control of the 2 phase signal 2P'. From state 8 it moves to state 11 under control of the signal 3P' and continues, under control of the signals 2P' and 3P', to run through the steps 15 and 16. The ring moves from state 15 to state 16 under control of the signal 2P'. As soon as it reaches state 16 it returns to state 7 under control of the signal 2P', and starts a new cycle. This step from state 16 to state 7 is under control of the signal marked SS1-220 on Figs. 4-57 and 4-63. The output SS1-220 remains connected to -45 V as long as one or more of the step switches have not returned to their home position. As soon as all four step switches are back in their home position, the output SS1-220 is connected to ground, and the step from state 16 to state 7 is not taken. Instead of rapidly moving through state 16 to state 7, the ring now remains standing in state 16. It will return to state 1 under control of the relays N1 and N2 as described at the end of this part.

The Step Switch Cycle controls the two selenium circuits PUB7 and PUN2, which pick up the relays B7 and N2, respectively. Every time the ring runs through the states 7 to 12, the relay B7 is picked up. The conditions for PUB7 and PUN2 are shown in Fig. 4-65 and Fig. 4-57, columns 24 and 25. The relay B7 applies pulses to the step switches through its contacts. The relay N2 is picked up when the ring remains standing in state 16 sufficiently long, that is, when all step switches are home, and the ring remains in state 16. Its function is described in Part L.

Next Line Cycle

When the relay contact M4-3' is connected to -45 V and the machine is stopped, the Main Control Ring will run through the Next Line Cycle. This cycle is used in connection with most of the manual controls. During 4 number time the ring steps from position 1 to position 6. During the following 3 number time it steps from position 6 to position 7, a step independent of the relay M4. If, on step 7, the Stop trigger pair is still in the state with S' low, the Step Switch Cycle will follow the Next Line Cycle immediately. However, if during the first step of the Next Line Cycle the Stop trigger pair output S has become low, it is not possible to continue the Step Switch Cycle from step 7 to step 8 since this requires S' to be low. Instead, the step from state 7 to state 16 can be taken under control of the output M-3. This is the "next line" match, and occurs four number times before the code corresponding to the number in the Line Number Register is to operate. A Call Cycle match occurs on step 8 of the Call Cycle, and four number times before the number time at which the code corresponding to the number in the Line Number Register is to operate. The time between the moment the next line match occurs and

the moment at which the ring arrives at state 1 is one number time longer than the corresponding time for the Call Cycle. Hence, the first code read when the ring arrives at state 1 is not the code corresponding to the number standing in the Line Number Register, but the code corresponding to a number one higher, and whereas the Call Cycle puts in control the code corresponding to the line number called, the Next Line Cycle puts in control the code corresponding to the next line number.

Specified Line Cycle

With -45 V applied through the relay contact M4-3, the Main Control Ring standing in state 1 will step to state 2 during 4 number time and, during 3 number time of the next phase, from state 2 to state 5. While the ring stands in state 2, the numbers stored in the Start Line Number strip switches are read out to the Fast In-Bus and into the Line Number Register during 2 number time (Fig. 4-57, column 17). This operation is controlled by the Main Control Ring and the relay output M4-3. The reading out of the Start Line Number is discussed more fully in Part L. While the ring stands on step 5, the state of the Stop trigger pair is changed, causing the output S to become low and to pick up the relay J1, so that the output K3-6' will be at -45 V. The ring will now follow the Call Cycle from step 5 to step 8 during 5 digit time following the application of the voltage. The ring continues the Call Cycle so that the first code to be read will be the code corresponding to the line number read in from the Start Line Number strip switches. As the relay J1 is picked up under control of the trigger pair S, it opens up the 100 V hold line to the relay M4, so that this relay will drop out. When the ring reaches state 1 at the end of the Call Cycle, the Specified Line Cycle cannot be repeated as the -45 V supply through M4-3 is then disconnected.

Record Cycle

The codes to be stored on the sequence section of the magnetic drum are read from a tape to the Fast In-Bus, then into the First Sequence Trigger Pairs, and they are subsequently recorded on the drum. The line number specifying the position on the drum where the code is to be stored is also recorded on the tape. The Record Cycle shown in column 7 of Fig. 4-57 provides the controls for: a) reading the line number from the tape into the Read Register; b) transferring the number from the Read Register into the Line Number Register; c) reading the code from the tape to the Read Register; and d) transferring the code to the First Sequence Trigger Pairs. The ring will step through the Record Cycle under control of the Sequence tape pushbuttons "Run," "Record" or "Read" (Fig. 4-2). Figure 4-56 shows that whenever these buttons are used, the relay K3 is picked up. Through the contact K3-3, -45 V is applied to various levels of the Main Control Ring, allowing it to step through the Record Cycle. At 4 number time the ring steps from state 1 to state 2. While it stands in this state, and during 1 number time, the "Read Tape" signal, RST, is given. In the following number time the ring steps from position 2 to position 3 so that this command will not be repeated. The ring remains waiting in position 3 until the "Busy" signal of the tape mechanism, RDB, becomes low. With RDB low, the ring steps from position 3 to position 4 during 0 number time. During the subsequent 1 number time, the number read from the tape is read out of the Read Register into the Line Number Register. This number should be a line number identified by its serial index. The absence of this index will cause a Stop command. Such a Stop command, which may also occur at state 6, does not cause the ring to stop immediately, and affects the Record Cycle only when it reaches state 6. After the line number has been

read into the Line Number Register at 1 number time, a command for reading the code from the tape is given at 2 number time. At 3 number time the ring steps to state 5, where it remains waiting until the "Read Busy" signal disappears; it then steps from state 5 to state 6 during 0 number time, and the code is read out of the Read Register into the First Sequence Trigger Pairs. At the end of 1 number time both the line number and the code are stored in their proper registers. Depending on which button has been pushed, the ring can now proceed in three different ways. With the "Run" button pushed the relay K3 will be picked up, but not relay K1. This makes the output K3-6 low. With the Stop trigger pair in the state where S is low, the ring will step from state 6 to state 1 during 2 number time and repeat the same cycle. The Run button therefore repeatedly reads line numbers and their associated codes from the tape into the proper registers without recording the codes on the drum or displaying them in the wheels. As the step from state 6 to state 1 requires the output S to be low, if it is high the step will be omitted and instead the ring will step from step 6 to step 7 at 3 number time, under control of the Next Line Cycle. This alternative is taken when the Read button is pushed or when a Stop is introduced during the Run or Record Cycle. From state 7 the Main Control Ring will now follow the Step Switch Cycle which controls the step switches used to display the numbers present in the Line Number Register and First Sequence Trigger Pairs in the indicators. In case the Record button is pushed, the step from state 6 to state 1 is omitted, this time not because the output S is high but rather because the relay K1 is picked up and disconnects the -45 V supply from the contact K3-6. The ring therefore again steps from state 6 to state 7 during 4 number time, but with the output S low. Consequently the ring continues to follow the Next Line Cycle and a match is obtained between the number in the Line

Number Register and the number time and phase. As mentioned in the description of the Next Line Cycle, this match occurs during number time M-4. During 12 digit time of number time M-2 the ring reaches state 15, and remains standing in this state until 10 digit time of the number time M-1. During 16 digit time of number time M-2 the command RR1 (Fig. 4-65) is obtained, and steps the Record Ring so that the code will be recorded during the cycle M-1. This part of the operation was described in Part D. The Main Control Ring continues to step through state 14 to state 1, where it resumes the Record Cycle. A further description of the manual controls involved in the recording and reading operation is given in Part L.

It can be seen from the previous discussion that all Main Control Ring cycles begin at state 1 of the ring, which is also the state in which the ring should stand when the machine is not in use. When power has been removed from the sequence circuits and is reapplied, the Main Control Ring would be standing in a random position, as would the Stop trigger pair. In order to remove such a possibility, the N1-3 contact of the relay N1 is used in the hold levels of the circuit for S and in the circuits for MCR4', MCR3', MCR2' and MCR1'. Whenever the machine is not in use, the relay N1 is not picked up. This disconnects the -45 V supply from the hold level of the circuits mentioned, forces the control ring to the state 0000, and forces trigger pair S to the state with S' low. This situation occurs also at the end of the Step Switch Cycle when the relay N2 is picked up, and in turn releases the hold of the relay N1. At the start of this operation the Main Control Ring is standing in state 16. As the relay N1 drops out, the ring steps to state 1, since level 1, the hold level of MCR4', becomes high. With the ring returned to state 1 the relay N2 is no longer picked up by the circuit PUN2.

K. Indicator Circuits

The layout of the indicators associated with the sequence mechanism is shown in Fig. 4-3. The upper two sets of indicators are each capable of displaying a 16-digit number with its sign. The lower set can display a 4-digit line number and a code written in the decimal form of eight digits. As mentioned in Part B, only one of the two sets of 16-digit indicators is associated with the sequence mechanism, the other being controlled by the tape control circuits. The selection between the two sets is made by the Upper-Lower toggle switch (Fig. 4-2). The set of indicators associated with the sequence mechanism can display the number which will be transferred under control of the code stored in the First Sequence Trigger Pairs. The line number and code indicators can display numbers standing in the Line Number Register and the First Sequence Trigger Pairs respectively.

The reading of numbers to indicators takes place in two steps. In the first, the information is read serially through step switches into a relay storage. The number remains stored in the relays as long as it is displayed in the indicators. A neon light is associated with each relay. The numbers are stored in the relays in their coded decimal form. The relays are pulled through vacuum tubes, which in turn are controlled by selenium circuits. In the second step of the transfer, the information is read in parallel from the relay storage to the indicators, again under control of step switches. The numbers are thus displayed twice, once in their coded decimal form by the neon lights of the relay storage, and once as decimal digits by the indicators.

Number Indicators

The reading of numbers to their indicators is initiated by the "Number" button shown in Fig. 4-63. The number to be read is determined

by the code stored in the First Sequence Trigger Pairs. This code will, in general, specify a number transfer. During the read operation the number to be transferred is read out and regenerated under control of the circuits CA, βCAR and γCAR (Fig. 4-49). The read-in, which may be specified by the code, is not performed. Under control of step switch 1 (Fig. 4-63) the sixteen digits and sign of the number are read in succession into the trigger pairs NRO (Fig. 4-40). Each digit of the number is stored in these trigger pairs long enough to allow a set of relays to pick up. Figure 4-66 shows these relays, which store the number to be displayed. The selection of the relays is performed by step switch 1. This step switch also determines the digit which is to be stored in the trigger pairs NRO. Finally the step switch controls the reset of the relay register prior to the read-in of the new number.

The operation of the trigger pairs NRO-8 - 1 is illustrated by the conditions for NRO-4 shown in Fig. 4-67. These circuits operate under control of the Step Switch Cycle of the Main Control Ring. Column 8 of Fig. 4-57 shows that on state 8 of the ring a digit can be read from the Fast In-Bus to the circuits NRO. At the same time the code advance is performed, which will cause the desired number to appear at the bus. The digit which is read in is selected by the signal Y DT'. This is one of the digit time signals 1 DT' - 17 DT' which are obtained through level 1 of step switch 1. The trigger pairs will hold through level 1. This level contains the conditions MCR 3' which will cause the trigger pair to reset on reaching state 15 of the ring. The trigger pair thus retains its information during states 8, 11 and 12 of the Step Switch Cycle. During this time the storage relay is pulled. During these states the circuit PUB7 also has a low output, which causes the relay B7 and the coil of step switch 1 to be energized.

It can be seen from Fig. 4-67, level 1, that the trigger pairs will hold only when the relay C1 is picked up. Thus the circuits can operate only when the Number button is pushed.

The number indicators are turned to the desired position by step switch 2. Figure 4-69 shows the number of pulses supplied to the indicators and the position of the digits on the wheel. The indicator used for the sign has no digits, but the symbols +, - and S. S is used to indicate a serial number. The operation of the indicators and their associated relay and step switch circuits as shown in Figs. 4-63 and 4-66 will not be discussed in detail.

Line Number and Code Indicators

All manually initiated operations of the sequence mechanism end with a display of both the line number and the code involved in the operation, in their respective indicators. The number standing in the Line Number Register and the code stored in the First Sequence Trigger Pairs are read out serially through the circuit LNCO (Fig. 4-40) to an intermediate relay storage (Fig. 4-70), and in parallel from this relay storage into the indicator wheels. The reading out of the line number and of the code from their trigger pairs is performed through step switch 3 (SS3) shown in Fig. 4-63. On step 2, the relay storage is reset. On steps 3-11, -45 V is delivered to the selenium circuits LNCO 8 - 1. The logical specifications of LNCO 8 are shown in Fig. 4-68. Each first level is controlled by a rectifier control and by its -45 V supply terminal. This terminal is connected either to ground or to -45 V by means of the contacts of step switch 3. Levels 1-5 are used for reading out the code digits. The digits of the number in the Line Number Register are read out through levels 6 - 11. For the unit's

ten's, and thousand's digit no transformation is necessary. For the hundred's digits, it is necessary to perform a translation from the outputs of the odd and even hundred's registers to the four relays which will store the hundred's digit. This translation is performed in the circuit LNCO by its levels 8, 9 and 10. The outputs of the selenium circuits are inverted and fed to cathode followers controlling puller tubes (Fig. 4-40). These tubes pick up the line number and code storage relays through the contacts of step switch 3.

The four decimal digits of the line number are stored in the same manner as the digits of a 16-digit number read from the machine. The code digits are directly stored in twenty relays, and the neon lights associated with each of these relays display the code in its binary form. Since the code is read in from the tape and by manual control in the form of eight decimal digits, it is desirable to display it in the indicator wheels in this form. This requires a translation from twenty binary digits to eight decimal digits. This translation is performed by the relay pyramids shown in Fig. 4-70.

L. Manual Controls

All manually controlled operations of the sequence mechanism are initiated by means of the buttons and switches on the Main Control Panel. The layout of this panel is shown in Fig. 4-2 and its functions are sketched in Part B. The buttons and switches control the relays shown in Figs. 4-56, 4-63, 4-66 and 4-73 through selenium rectifiers. The functions of the relays are the following:

1) They control the switches and buttons of the front panel. Such control is necessary to prevent the initiation of a new operation while a previous operation is still being performed, and to prevent the repeated performance of an operation when the controlling button is held down too long.

2) They control the sequence cycling circuits, mainly through the selenium circuits of the sequence mechanism.

Interference

The circuits which prevent the initiation of a new operation while a previous one is still being performed make use of the interference relay N1 shown in Fig. 4-56. This relay is picked up whenever the machine is engaged in an operation; it is not picked up when the machine is not being operated. In the latter case, it applies 100 V through the contact N1-2' and level 2 of step switch 4 (Fig. 4-73) to the line marked "Start" (Fig. 4-56). All pushbuttons, with the exception of the Stop pushbutton and the line number and code Reset pushbutton are connected to the Start line. When the machine is not busy, the 100 V supply is connected to this line and can be connected, by pushing any of the buttons, to the relays associated with this button. The relay thus picked up holds itself through its contact 1 to one of the four hold lines, Hold 1, Hold 2, Hold 3 or Hold 4. One or more

relays, depending on the button pushed, will pick up relay N1 via their contact 4, and relay N1 then holds itself through contact N1-1 to the Hold 1 line. If another button is pushed no more relays can be picked up, since the 100 V supply is now disconnected from the Start line by relay N1. When the relay N2 is picked up, at the end of the operation, the 100 V supply will be disconnected from the Hold 1 line making relay N1 drop out. This marks the end of the operation.

The relay N1 is also used in the timing of the manually controlled operations. Since it is picked up through the contacts of the relays controlled by the buttons, it is energized later than these. The -45 V supply which controls the Main Control Ring cycling is connected through the contact N1-3 to the contacts of the relays K1, K3, and M4. Because relay N1 is picked up late, the contacts of K1, K3 and M4 will be in the desired position before the -45 V supply is connected, preventing ambiguity in the initiation of the Main Control Ring cycles.

Button Return

A second control common to all pushbuttons is the Button Return. This control makes use of the relay N2 (Fig. 4-56). At the end of every operation, the Main Control Ring is standing in state 16, and the output of the circuit PUN2 (Fig. 4-65) is low if the -45 V supply is connected to terminal 1 of this circuit. This voltage will be present provided that the machine is stopped, and the step switches 1, 2, and 3 are home. A low output of PUN2, when inverted, gives a high voltage to the 2C51 puller tube. This tube will pick up the relay N2, provided its 150 V plate supply is connected. This connection is made only when all the pushbuttons are returned, and their normally closed contact is made. The connecting path may be traced through the buttons of Fig. 4-56, Fig. 4-73, and Fig. 4-63.

When relay N2 is picked up, it disconnects the 100 V supply from the Hold 1 line. The Hold 1 line in turn feeds the Hold 2 line through the contact C3-1', and the Hold 3 line through the contact V6-1'. Relays C3 and V6 are picked up during the operation of step switch 1 and step switch 3, respectively. The Hold 2 and Hold 3 lines are thus disconnected from the 100 V supply before the Hold 1 line is disconnected. A fourth hold line, Hold 4, is provided through the contact J1-1'. This hold line will be disconnected as soon as the output S becomes low. This occurs before the operation of the step switches, hence before Hold 2 or Hold 3 are disconnected. In Fig. 4-77 the pushbuttons of the Main Control Panel are listed, together with the relays picked up under control of these buttons.

Read-In Switch

The Read-In Switch consists of sixteen ten-position strip switches for the 16 decimal digits of the number to be read in, and of one two-position strip switch for the sign. The strip switches are shown schematically in Fig. 4-71. For each button, three normally open contacts are used. One is used for a continuity check, and two are used to specify the number selected. This is accomplished by connecting one or two of four wires marked 8, 4, 2 and 1 to a -45 V supply. The connections are made according to the number system which is used in transferring numbers along the bus. Four output wires are controlled by each of the strip switches. These outputs are fed into selenium scanning circuits MCO. The circuits for the 8, 4, 2 and 1 wires all use the same selenium circuit of type E12 (Fig. 4-84). Figure 4-72 shows the logical conditions for MCO-8 which combines the 8-wires of the manual controls. Levels 1-16 are used to read out the sixteen decimal

digits set in the Read-In Switch. The -45 V supply for each of these first levels is provided through the contacts of the strip switches. Levels 1-16 are controlled by the signal RIS' which will be low whenever a read-out from the Read-In Switch is desired. In this case, the unit's digit is read out during 0 digit time, the ten's digit during 1 digit time, etc. The read-out is thus performed with the same timing as the read-out of the Line Number Register, the Slow Storage Control Register, and the I, J, K Register. A low output of a circuit MCO is inverted and fed into a cathode follower connected to the same cathode resistor as the cathode followers of LNRO, IJKRO, and SCRO (Fig. 4-46). This output then goes to the Regeneration Circuit as described in Part F. The two-position strip switch for the sign also connects to the 8, 4, 2 and 1 wires which feed the MCO circuits on level 24. This level is controlled by the signals RIS' and 19 DT'. When the plus button is pushed, none of the four wires is connected to -45 V. If the minus button is pushed, the 8-wire supplies -45 V to level 24 of MCO-8. If both the plus and minus buttons are pushed, -45 V is connected to level 24 of the circuits MCO-4, MCO-2, and MCO-1. The binary configuration of the output in this case is 0111, the code for the serial index S. Figure 4-74 shows the conditions for the circuits RIS'. This circuit is low for the α code, "Read-In Switch Out."

Sign Register

Figure 4-71 shows the toggle switch used as Sign Register. The operation of this switch is similar to that of the strip switches. When the switch is thrown, it connects -45 V to level 23 of the circuit MCO-8. This level is low during 19 digit time under control of code β3332. The sign is read out onto the Fast Out-Bus during 0 digit time. The Sign

Register can be used for several purposes. It can be used to control a conditional call, making it possible to control a routine from the Main Control Panel. When ganged numbers are used, the Sign Register is used to indicate whether the decimal point is located in the upper or in the lower sixteen decimal digits of the number.

Decimal Point

The decimal point strip switch (DPS, Fig. 4-71) is used to control the decimal point selection. In addition, it may be read out to the Fast Out-Bus and Fast In-Bus. This read-out again is accomplished through the circuits MCO-8 - MCO-1. The switch indicates the number of digits to the right of the decimal point and therefore can be set to a number in the range 0-16. The unit's digit again is read out to the Regeneration Circuit during 0 digit time. This is performed on level 22 of the circuits MCO-8 - MCO-1 under control of the code β3333. The ten's digit is read out during 1 digit time under control of the same code.

Upper-Lower Indicators

The selection between the upper and lower sets of number indicators is made by the Upper-Lower toggle switch (Fig. 4-66). This switch can connect the 100 V supply to the coils of the relays B1-B6. The storage relays are connected to the upper indicator wheels through the normally closed contacts of the relays B1-B6. Only one of the upper wheels has been included in Fig. 4-66. When the relays B1-B6 are energized, the storage relays are connected to the lower set of wheels. The Upper-Lower toggle switch is used to read numbers from the bus into two sets of indicators for comparison.

Number

The number to be transferred by the code standing in the First Sequence Trigger Pairs may be read into the indicators under control of the Number button (Fig. 4-63). When the Number button is pushed, relay C1 is picked up. This, in turn, picks up the relay N1. The relay N1 now is held by contact N1-1, and the -45 V supply is connected to the output M4-3'. This output is used in the Next Line Cycle of the Main Control Ring; it steps the ring from state 1 to state 6 during 4 number time. During the following 3 number time the ring advances to state 7. Since the relay J1 is not energized, the ring starts on the Step Switch Cycle. During this cycle, while the ring is standing in state 8, the code is advanced during 2 number time and a digit of the number, which is transferred, is read into the trigger pairs NRO. This has been described in Part K. While the step switch coil is energized this digit is read into the storage relays. On step 15 of the ring, the relay B7 is no longer energized and the step switch is advanced. At this moment, the trigger pairs NRO8-1 are again reset. As long as step switch 1 and step switch 2 have not returned to their home position, the -45 V supply is connected to the circuit of MCR3' so that when the ring reaches state 16 it will step to state 7. When both step switches are home, the relay N2 is picked up while the ring is waiting in state 16. Finally, the relay N1 is dropped out as previously described.

Reset

The Reset button (Fig. 4-63) which is grouped with the Number button resets the indicator selected by the Upper-Lower toggle switch. The Reset button picks up the relay C6. When the relay N1 is picked up through contact C6-4, the Next Line Cycle is initiated. The same operations are

performed as with the relay C1 picked up except that the -45 V is not connected to the circuits CA and NRO8-1 so that no new number is read into the storage relays. Thus all the digit indicator wheels are reset and remain in their blank positions. Step switch 2 does not move during this operation.

Start Line Number

The Start Line Number strip switches (Fig. 4-71) are used to indicate the number referred to by the Specified Line buttons for "Start," "1 Line" and "Read." These buttons pick up the relay M4 and start the Main Control Ring with the Specified Line Cycle. The operation of the switches is similar to that of the Read-In Switch. Levels 17, 18, 19, and 20 of the circuits MCO are used to scan the strip switches, under control of the digit time and the outputs MCR4 and MCR1' of the Main Control Ring. The -45 V supply is not connected directly to the Start Line Number strip switches, but is first sent through the contact M4-3. The Main Control Ring has four states in which the combination MCR4, MCR1' occurs, namely, states 2, 3, 4, and 5. However, states 3 and 4 are not used in the Specified Line Cycle. The start line number is read out during 2 number time at state 2. The ring steps to state 5 during 3 number time. It is possible for the start line number to be read to the Fast Out-Bus again during 2 number time while the ring is standing on state 5. During this time, however, the Line Number Register cannot read in, hence this operation does not conflict with any other being performed at the time.

When a button belonging to the Specified Line group is pushed, the relays M4, M3 and N1 are picked up in succession. Relay N1 connects the -45 V supply to the contact M4-3. As a result, the Main Control Ring

is started on its Specified Line Cycle. The relay M4 is held on the Hold 4 line. At state 5 of the Specified Line Cycle the output S is made low under control of the contact M3-3 (Fig. 4-57, column 16). The relay J1 is picked up, disconnecting the Hold 4 line, and causing the relay M4 to drop out. The machine now proceeds with the operation determined by the other relays which were picked up simultaneously with the relay M4, when a button of the Specified Line group was pushed.

One Line

When a One Line button (Fig. 4-56) is pushed the relay M3 is picked up. This occurs either directly, when the button belongs to the Next Line group, or through the relay M4, when the button belongs to the Specified Line group. The contact M3-4 in turn picks up the relay N1. Contact N1-3 connects the -45 V supply to the output M4-3 and M4-3'. If the relay M4 has been picked up, the Main Control Ring starts on the Specified Line Cycle; if not, the Next Line Cycle is started.

In the Specified Line Cycle, signal S is produced at state 5. As soon as the relay J1 is picked up, the control ring follows the Call Cycle, which, when completed, puts into operation the code corresponding to the line number specified. The Main Control Ring reaches state 1 during 8 digit time of the number time preceding that in which the code is to operate. During 1 digit time of the following number time a stop signal is produced under control of M1-6'. This stop signal occurs after the code advance signal, so that the specified code has already been advanced. The ring now proceeds with the Stop Cycle, moves from state 1 to state 7, and then starts the Step Switch Cycle. This procedure reads the number in the Line Number Register and the code just performed into the corresponding indicators.

When the One Line button of the Next Line group has been pushed, the Main Control Ring starts on the Next Line Cycle (Fig. 4-57, column 5). In this cycle the ring steps from state 1 to state 6, and while it stands in state 6 the output S is made low during 2 number time. The ring continues in the Next Line Cycle as soon as the relay J1 has been picked up, and follows the Next Line Cycle and the Call Cycle described in Part J. When the ring returns to state 1 the desired code is advanced into the Second Sequence Trigger Pairs. A stop signal occurs at the following 1 digit time, and the Step Switch Cycle proceeds. The contact M3-2 feeds the pulses produced by the relay B7 to the coil of step switch 3. When the ring starts on the Step Switch Cycle at the end of a One Line operation, step switch 3 is advanced and causes the Step Switch Cycle to continue until both step switch 3 and step switch 2 are in their home position. By this time, the performed code and its line number will have been read through the storage relays into the indicators. If it is not desired to read the line number and code to the indicators, the Step Switch Cycle can be omitted by throwing the Indicators toggle switch. This disconnects the 100 V pulses produced by contact B7-1 from the coil of step switch 3. Thus when the Main Control Ring has stepped from state 7 to state 16 both step switch 2 and step switch 3 are home. The relay N2 is picked up and causes the relay N1 to drop out, finishing the operation.

Read

The Next Line Read button (Fig. 4-56) picks up relay M2. This relay picks up the relay M3. The relay M3 in turn causes the machine to run through the same cycle as that performed under control of the One Line button, except that the contact M2-4 disconnects the -45 V supply from the Code Advance circuit (Fig. 4-49) so that no code can be advanced to the

Secord Sequence Trigger Pairs. In addition, any I, J, K, or Conditional Call control is prevented from operating.

When the Specified Line Read button is pushed, both relays M2 and M4 are picked up. The ring now starts on the Specified Line Cycle as described in the One Line operation, with the reservation mentioned above.

Start

The Next Line Start button (Fig. 4-56) energizes the relay M1, which in turn picks up the relay M3. The ring is started again on the Next Line Cycle through the contacts of M3 and performs the same operations as when the One Line button was pushed. However, contact M1-4 connects the hold contact of the relay M3 to the Hold 4 line instead of the Hold 3 line. As the relay J1 is picked up, when the output S becomes low, it disconnects the Hold 4 line, causing the relay M3 to drop out. Moreover when the ring returns to state 1 after the match has occurred, the stop operation which would proceed under control of the contact M1-6' does not, and the machine continues to run. If the Specified Line Start button is pushed the ring starts on the Specified Line Cycle. At state 5, when the output S becomes low, the relay M3 drops out, since the Hold 4 line is opened.

While the machine is running, the relays M1 and N1 are picked up. Whenever a Stop occurs, the ring steps through the Stop Cycle and begins the Step Switch Cycle. As step switch 3 steps from state 13 to state 14, the -45 V supply line which is fed through J1-1' and level 2 of step switches 1, 2, and 3 to MCR3', is opened by contact M1-3. The ring therefore gets stuck in state 16, step switch 3 remains standing on step 14, and step switch 2 on step 6. As step switch 2 is standing on step 6, the 100 V supply is connected through contact M1-1 to the coil of the relay

J3. Contact J3-1 in turn closes a circuit through the Alarm Bell, which rings until step switch 2 leaves this position. Step switches 2 and 3 are moved under control of the Bell button which provides an alternate path for the -45 V supply to MCR3', so that the ring can move on and consequently also advance step switch 2. The Step Switch Cycle can now be completed in the usual manner, returning the ring to state 1. In the case that the machine is stopped by means of the Stop button the relay contact J2-5 will provide the path for the -45 V supply, thus preventing the operation of the Alarm Bell.

Stop

The Stop button (Fig. 4-56) may be pushed at any moment. This button connects 100 V to the coil of relay J2. When the machine is running, the relay N1 has already been picked up. In this case the purpose of the relay J2 is to connect the -45 V supply to levels 8 and 9 of S', producing a stop when the Main Control Ring stands in states 1, 7 or 8. The Main Control Ring then steps through the Stop Cycle, followed by the Step Switch Cycle, finally displaying the line number and code at which the machine has stopped. When the Stop button is pushed while the machine is stopped, the relay J2 picks up the relay N1, starting the ring through the Next Line Cycle. This cycle is followed by the Step Switch Cycle. Step switch 3 is advanced through contact J2-6 under control of this cycle, to display the number in the Line Number Register and the code in the First Sequence Trigger Pairs in their indicators. This makes it possible to read to these indicators at any desired moment.

Specified Line Stop

The Specified Line Stop toggle switch (Fig. 4-56) is used together with the Stop Line Number strip switches. The purpose of this switch is to

stop the calculator when the Line Number Register stores the number which has been placed in the Stop Line Number strip switches. The outputs of these strip switches are indicated in Fig. 4-71. The outputs are sent to the Stop Match circuit (Fig. 4-56 and Fig. 4-75) where they are compared with the outputs of the Line Number Register. The selenium card Ell which performs this comparison is shown in Fig. 4-83. The circuit is a twenty-five first level selenium circuit whose output is low whenever one of the twenty-five levels is low. The output of a first level in the circuit Ell can be high either because of a high input from the Line Number Register, or because the strip switch puts the level at ground potential. When the outputs of the Line Number Register and the strip switches match, the output of every first level is high. In this case, the wires coming from the strip switches ground those levels that have low inputs from the Line Number Register, while the other levels are high because of the high inputs from the Line Number Register. Hence a high output SM indicates a match. For each of the unit's, the ten's, and the thousand's digits stored in the Line Number Register two out of five trigger pair outputs are low, and the other three outputs are high. For the hundred's digit two out of the ten outputs are low and the others high. The output of the circuit SM is inverted and sent to the Stop trigger pair. Level 5 of Figure 4-62 shows that the Stop trigger pair will operate under control of SM when -45 V is supplied through the Stop toggle switch. During 0 digit time of the cycle in which the output is low, the output S' becomes low and the Main Control Ring begins the Stop Cycle. This cycle again is followed by the Step Switch Cycle as described in Part J and earlier in this Part. The matching circuit has been so connected that when no button is pushed in one or more of the strip switches, no match can occur. To give a warning of this occurrence, a

check has been included which lights an indicator light whenever one of the columns of the Stop Line Number is blank.

Line Number

The ten buttons marked Line Number (Fig. 4-73) are used to read numbers into the Line Number Register. The ten buttons connect the 100 V supply through a selenium rectifier matrix to four relays marked V8, V4, V2, and V1. The selenium matrix translates the decimal digit of the button pushed into its coded decimal equivalent. The outputs of contact 3 of the relays V8-V1 are fed to the circuits MCO-8 - MCO-1 on level 21 (Fig. 4-72). The digit is then read from the circuits MCO-8 - MCO-1 to the bus and into the Line Number Register. This operation is controlled by the Main Control Ring and step switch 4. The Main Control Ring controls the cycle during which the digits are read into the Line Number Register. The step switch controls the digit time, in this cycle, during which the number is to be read onto the bus. Step switch 4 consists of two identical parts of ten steps each, steps 1-10 and 11-20. The relays V8-V1 serve for both the read-in of a line number and the read-in of a code. When a line number is read in, the relay V3 is picked up. The relay V5 is picked up for the read-in of a code. In order to read in a complete line number, the line number buttons must be pushed four times. The first digit read in is the thousand's digit. The line number button which is pushed picks up one or two of the relays V8-V1, and the relay V3, by means of the rectifier matrix. Those among the relays V8-V1 which are energized pick up the relay N1, which starts the Main Control Ring on the Next Line Cycle. At state 6 of this cycle the Line Number Register is reset and the thousand's digit read in during 5 digit time. The digit time and state 6 of the Main Control Ring control

level 21 of the circuit MCO. This level can also be low at state 5 of the Main Control Ring. However, the Next Line Cycle does not go through state 5. The digit time is indicated in the circuit MCO by XDT'. It is determined by level 4 of step switch 4. The home position of step switch 4 also controls the reset of the Line Number Register. Contact V5-3 connects the -45 V supply through the step switch contact 601 to the circuits R, RO, REH, and RETH which, together with a low signal LNRRI', reset the Line Number Register. This reset and the read-in are controlled by level 2 of the circuit LNRRI'. The Main Control Ring proceeds from state 7 through the Step Switch Cycle. During this cycle, the relay B7 will apply a 100 V pulse to the coil of step switch 4 through the contact V3-2. Step switch 4 therefore steps after the read-in operation into the Line Number Register has been performed. The Main Control Ring will be returned to state 1 after relay N2 has released relay N1. As step switch 4 moves from position 1 to position 2 it connects the 100 V supply through its level 1 to the hold level of the relays V5 and V3. Thus the relay V3 remains energized even though the relay N1 has dropped out. After one digit of the line number has been read in, no other operation can be performed until either the complete line number has been read in or the step switch has been reset by means of the Reset button.

The hundred's digit is read in after the thousand's digit. No resets occur during this step since step switch 4 is no longer standing in its home position. The ten's digit is read in with step switch 4 standing on step 3, and when the unit's digit is read in, the switch is standing on step 4. As the relay B7 is picked up it connects the 100 V supply to the coil of step switch 4. At the same time, the coil of step switch 3 is energized. Step switches 3 and 4 continue to step together, until step

switch 4 has reached its second home position on step 11. Step switch 3 and step switch 2 complete their regular cycle and read the new line number and the unaltered code into the indicators. When both a line number and a code are to be read in, it may be desirable to omit the operation of the indicators between the read-in of the line number and the read-in of the code. This can be done under control of the Indicators toggle switch, which prevents the read-in to the indicators after the read-in of the line number.

Code

The read-in of a code is similar to the read-in of a line number. The relays V8-V1 are used again to indicate the digit selected. In this operation the relay V5 is picked up and held instead of relay V3. To complete the read-in of a regular code, the code buttons must be pushed eight times. Step switch 4 again is stepped under control of the Main Control Ring, as the digits are read through the MCO circuits to the First Sequence Trigger Pairs. Levels 1, 2, 4, 6, 7 and 8 of step switch 4 are used in reading in a line number, and levels 1, 2, 3, 5, 7 and 8 are used for code read-in. The signals XDT' which are used for reading out of the MCO circuits onto the bus are supplied through level 3 of step switch 4. The First Sequence Trigger Pairs are reset by means of the circuit FSR, to which the -45 V supply is connected through contact 501 of step switch 4. The reset thus occurs only when the step switch is standing in step 1 (or 11). Step switch 3 is energized on step 8 of step switch 4. At this time all eight code digits will have been read in and a cycle identical to that of the line number read-in occurs.

Special controls have been introduced through level 5 of step switch 4 for the read-in of the β thousand's digit and for the external

transfer operation. The β thousand's digit is read in to the L and M trigger pairs on step 3 of step switch 4. Figure 4-76 shows the logical specifications of the M trigger pair. Level 2 of MCTR' is used for the read-in from the drum. Levels 2 and 3 of MCTR are used for the reset preceding and following this read-in. The read-in from the Fast In-Bus is performed on level 3 of MCTR' under control of the signal FSRI'. The outputs of the circuits LCTR' and MCTR' for decimal digits 0, 1, 2 or 3, are shown in Fig. 4-28. When the output MCTR' is low, it changes the β unit's digit during 8-11 digit times. It can be seen from the conditions for FSTP11' - FSTP14' (Figs. 4-30 - 4-33) that a low signal MCTR' does not change the outputs of these trigger pairs when all four are reset. Thus when the signal FSRI' is low, on steps 3, 4 and 5 of step switch 4, the outputs of the trigger pairs FSTP11' - FSTP14' remain 0000. The β unit's digit is read in at 6 digit time, at step 6 of step switch 4. During digit times 8 to 11 following this read-in, the outputs of the trigger pairs FSTP11' - FSTP14' are changed under control of MCTR'. During 12 digit time of this cycle the MCTR trigger pair is reset under control of -45 V supplied through contact 506 of step switch 4. The control of FSTP7' - FSTP10' by LCTR' takes place in a similar way at step 5 of step switch 4. Contact SS4-505 connects the -45 V supply to the reset level of LCTR.

As described in Part H, the α code for an external transfer command is 04 or 05. The β and γ code digits are used to represent the four-digit number which is to be externally transferred. In the manual read-in of such a code, the α code digits are read in first, followed by the four decimal digits of the number, and the code buttons are pushed only six times instead of eight times as for a regular code. The α code indicating an external transfer is read in in standard fashion. This

external transfer code will be standing in the α First Sequence Trigger Pairs as the Main Control Ring starts on the Step Switch Cycle. At the end of this cycle, which moves step switch 4 from step 2 to step 3, the contact SS4-503 is made, applying -45 V to level 5 of MCR3'. With the output XT' low because of the code standing in the First Sequence Trigger Pairs, this level causes the Main Control Ring to step from state 16 to state 7, repeating the Step Switch Cycle. This cycle moves the step switch from step 3 to step 4. On this step the contact 504 is made, again applying -45 V to level 5 of MCR3'. Thus the same operation is repeated, and the step switch moves to step 5, after which the relay N2 is picked up and the step switch remains waiting until another code button is pushed. In this operation, the step switch passes through steps 3 and 4, without read-in to the First Sequence Trigger Pairs, and then stands ready for the read-in of the β ten's digit. The thousand's digit of the number to be externally transferred is read in to First Sequence Trigger Pairs 11-14 on step 5 of step switch 4, in the same manner as the β ten's digit of a regular code. The hundred's digit is read in place of the β unit's digit of a regular code. The ten's and unit's digits are read in on step 7 and step 8. With the output of the circuit XT' low, these read-ins are performed differently from the read-in of the γ ten's and unit's digits. The translation is made by the First Sequence Trigger Pairs 5', 6' and 15' - 20'. The rest of the operation is identical to that of the regular code read-in. The external transfer light will be lighted as soon as the output XT' becomes low and thus indicates that the read-in is different from a regular code read-in. The light also indicates that only the α digits of the number in the indicators are correct code digits.

Reset

The Reset button (Fig. 4-56) placed underneath the line number and code read-in buttons is used to reset the line number and code indicators and to reset step switch 4 in case of an incomplete read-in. The Reset button is independent of the Start line, but its start voltage is controlled by the relay J1-2 so that it cannot be used while the machine is running. It can be used, however, when step switch 4 is moved from either home position. The Reset button picks up the relays X2, X3, and N1, which start the Main Control Ring on the Next Line Cycle. At state 7 the Step Switch Cycle takes command and step switch 3 starts from its home position to position 2. When step switch 4 is not standing in position 1 or 11, it will move together with step switch 3. This returns step switch 4 to its home position in case of an incomplete read-in of a line number or a code. The wheels are reset to their blank position.

Operate

A code standing in the First Sequence Trigger Pairs can be performed under control of the Operate button (Fig. 4-56). This button starts the Main Control Ring on the Next Line Cycle by means of the relays X1 and N1. Column 21 of Fig. 4-57 shows that at state 6 of this cycle a code advance signal is given through level 1 of the circuit CA (Fig. 4-49) allowing a code advance during 18 digit time of 1 number time. The I, J, K and conditional call controls can operate with -45 V supplied through contact X1-3. Thus when the code standing in the First Sequence Trigger Pairs has an I, J, or K control the number in the I, J or K Register will be substituted as described in Part F. This occurs before the code advance signal is given at state 6 of the Main Control Ring. Following the Next

Line Cycle, the Step Switch Cycle is used again to read the line number and code into the indicators. The read-in to the indicator wheels is optional, and can be prevented by the indicators toggle switch.

Repeat

The Repeat button (Fig. 4-56) may be used to advance the code standing in the First Sequence Trigger Pairs to the Second Sequence Trigger Pairs during successive cycles; this is intended to be a testing control only. The operation is performed in level 3 of circuit CA (Fig. 4-49) to which the -45 V supply is connected through contact 3 of relay X4 and through the contact N1-3'. When the Repeat button is pushed X4 is energized and holds through its contact X4-1. If another button is pushed, the relay N1 is picked up and stops the Repeat operation. The relay X4 remains picked up but is non-operative. X4 is reset at the end of the new operation. A light indicates when a Repeat operation is performed.

Record

The Record button (Fig. 4-56) placed underneath the line number and code read-in buttons can be used to record the code standing in the First Sequence Trigger Pairs at a location on the drum determined by the number in the Line Number Register. When this button is pushed, it picks up the relays K1 and M3, thus starting the Next Line Cycle. At state 6 of the Next Line Cycle a signal S is given under control of the relay M3. When the relay J1 is picked up the Main Control Ring continues on the Next Line Cycle followed by the Call Cycle. At state 15 the circuit RR1 (Fig. 4-65) operates under control of the relay K1 so that the code will be recorded on the drum in the place determined by the line number, as described in Part J. The Main Control Ring returns to state 1, at which

point a Stop is produced under control of M1-6' as shown in column 23 of Fig. 4-57. The ring now proceeds on the Stop Cycle followed by the Step Switch Cycle thus reading the recorded code and its line number to the indicators.

Read Sequence Tape

The Read button (Fig. 4-56) is used to read one line number and its associated code from the sequence tape. As the button is pushed, the relay K3 is picked up. The relay K3 picks up relay N1, and then the -45 V supply is connected to contact K3-3. This starts the Main Control Ring on the Record Cycle shown in column 7 of Fig. 4-57. The Record Cycle will: 1) read from tape mechanism 1; 2) read out of Read Register 1 to the Line Number Register; 3) read from the tape mechanism again, and 4) read the next number from the Read Register into the First Sequence Trigger Pairs. With the output S' low, the ring now starts on the Step Switch Cycle and reads the line number and the code read from the tape into the indicators.

Run Sequence Tape

The Run button (Fig. 4-56) allows the sequence mechanism to read the sequence tape to check for the proper order of line numbers and codes and to stop under control of the Stop Specified Line toggle switch at a selected line number. When the Run button is pushed, it picks up relays K3, M1 and M3. After N1 is picked up, the contact K3-3 is connected to the -45 V supply, and the Main Control Ring starts on the Record Cycle. At state 3 of the Record Cycle, a signal which makes the output S low is given under control of contact M3-3. This in turn picks up the relay J1, disconnecting the Hold 4 line, and dropping out relay M3. The Main Control Ring continues to follow the Record Cycle through states 4-6. From state 6

it returns to state 1 under control of the -45 V supply connected through contact K3-6. The ring repeats the Record Cycle until the signal S' becomes low, after which the Step Switch Cycle follows.

Record from Sequence Tape

When the Record button (Fig. 4-56) is pushed, it picks up relays K3, K1 and M1. This results in the same series of operations as performed under control of the Run button. However, a different course is followed at state 6 of the Record Cycle. With the relay K1 picked up, the output K3-6 is no longer at -45 V and the ring follows the Next Line Cycle and the Call Cycle instead of repeating the Record Cycle. The code is recorded during the Call Cycle. At the end of this cycle the Main Control Ring returns to state 1 and then repeats the Record Cycle. This operation is stopped when the signal S' becomes low, as described for the Run button.

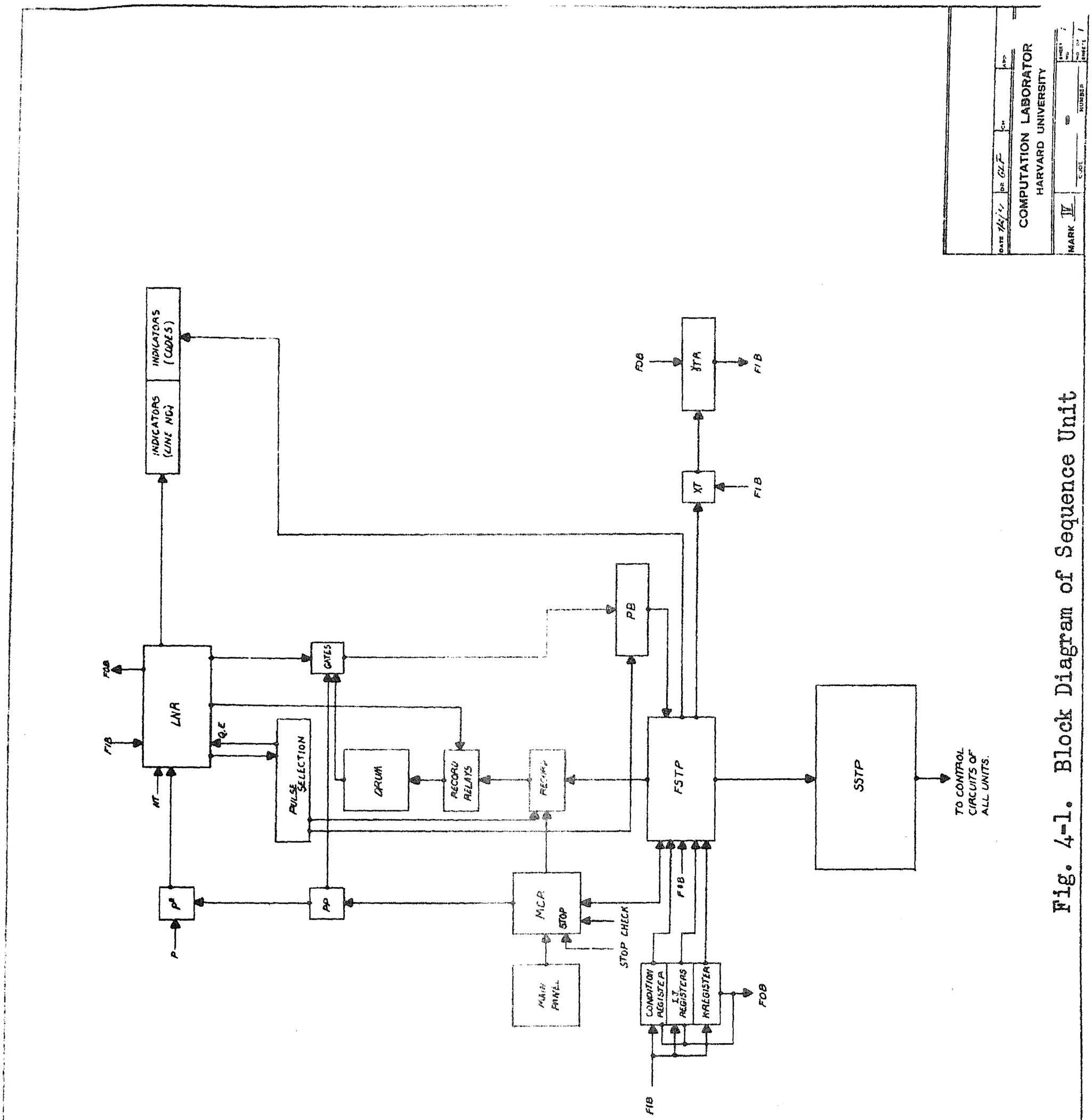


Fig. 4-1. Block Diagram of Sequence Unit

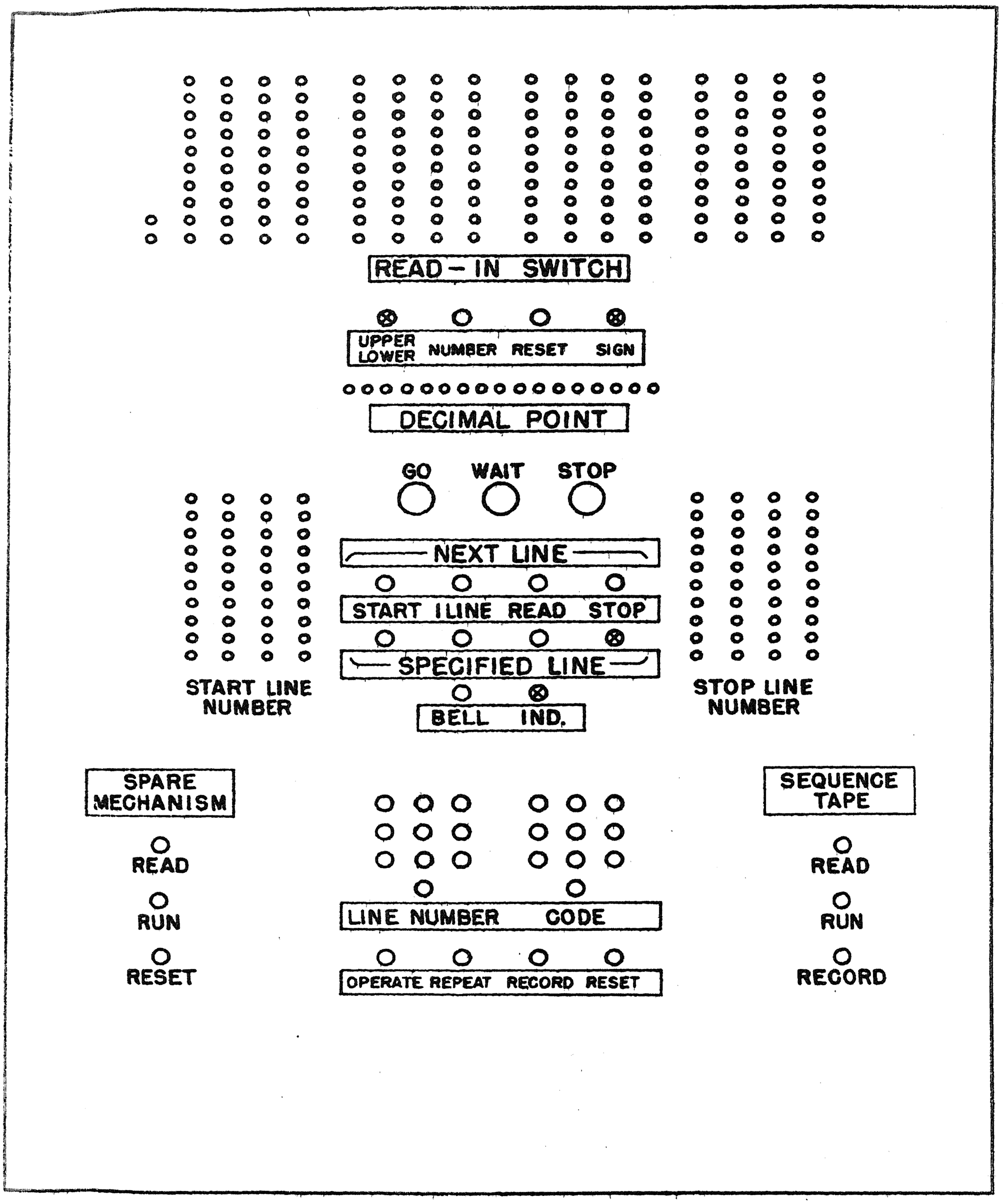


Fig. 4-2. Main Control Panel

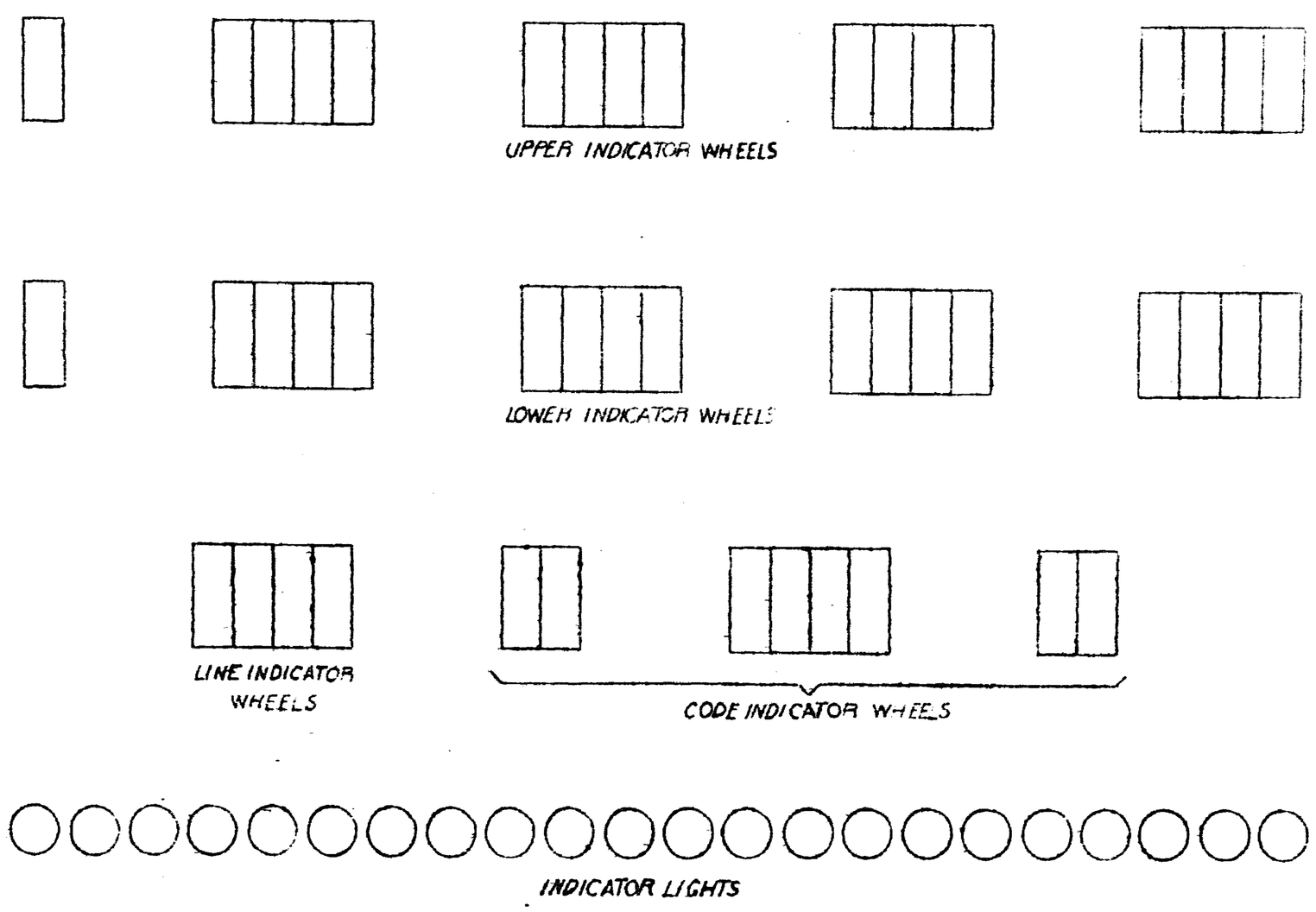


Fig. 4-3. Indicator Panel

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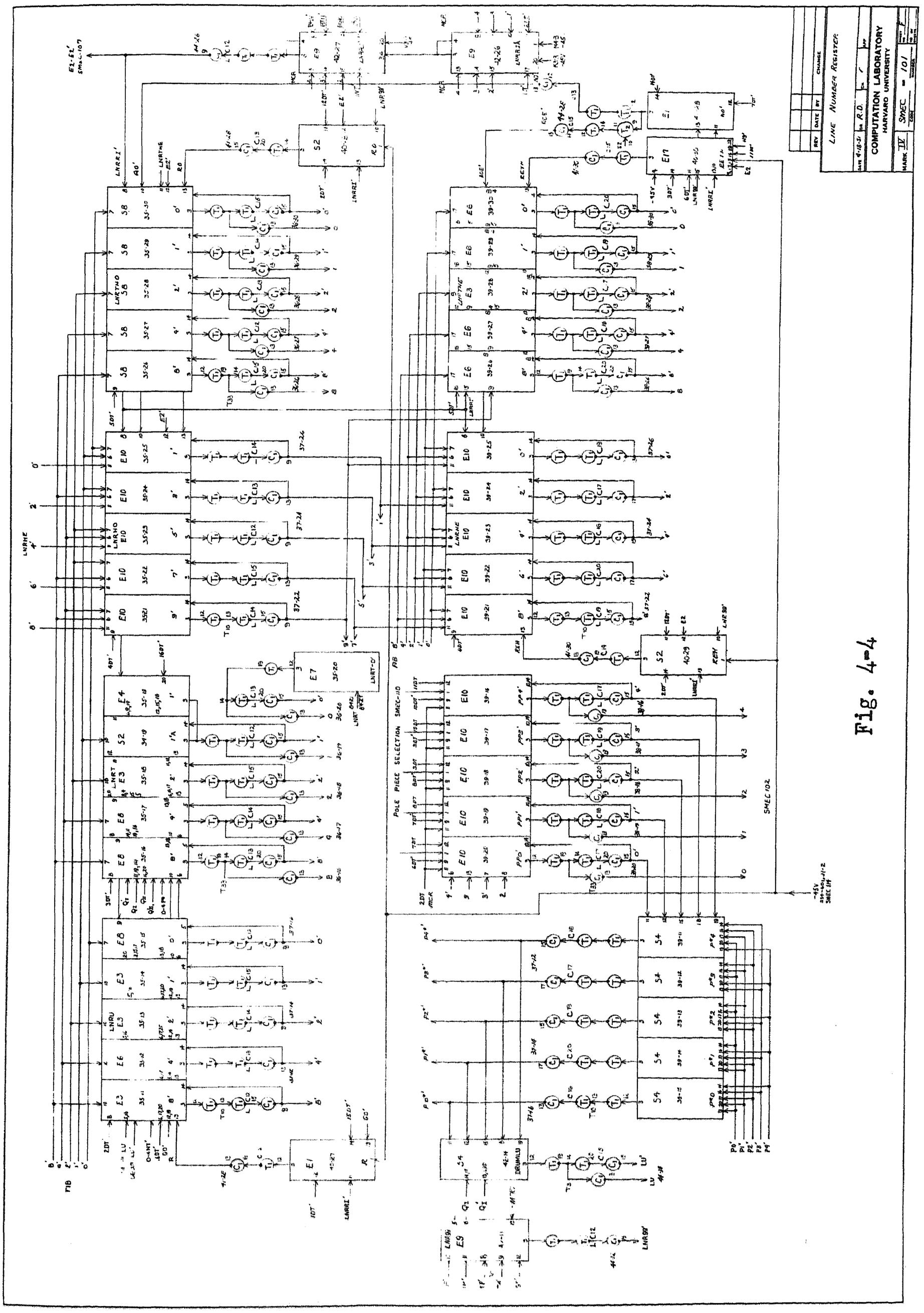

LINE NUMBER REGISTER
COMPUTATION LABORATORY
HARVARD UNIVERSITY
MARK IV SMEC - 101
POLE PIECE SELECTION SMEC-110
SMEC 102

Fig. 4-4

		1234	2987
LNRU	8'	0	1
	4'	1	0
	2'	0	1
	1'	0	0
	0'	1	0
LNRT	8'	1	1
	4'	0	0
	2'	0	0
	1'	1	0
	0'	0	1
LNRHO	9'	0	1
	7'	0	0
	5'	0	0
	3'	1	0
	1'	0	0
LNRHE	8'	0	0
	6'	0	0
	4'	0	0
	2'	1	0
	0'	0	1
LNRTHO	8'	0	0
	4'	0	0
	2'	0	1
	1'	1	0
	0'	1	1
LNRTHE	8'	0	1
	4'	0	0
	2'	0	0
	1'	1	1
	0'	1	0

Number Storage in LNR

Fig. 4-5

R Type E1 SMEC-101

1.	new no.	LNRRI';	1DT'			-45 V	SS4-601	
		11	12			1	J1-2	
2.	internal	GO';	15DT'				SMEC-114	
		13	14					

RO Type S2 SMEC-101

1.	new no.	LNRRI';	2DT'			-45 V	SS4-601	
		13	14			1	J1-2	
2.	internal	LNR99';	12DT';	E2'			SMEC-114	
		10	11	12				

REH Type S2 SMEC-101

1.	new no.	LNRRI';	2DT'			-45 V	SS4-601	
		13	14			1	J1-2	
2.	internal	LNR99';	12DT';	E2			SMEC-114	
		10	11	12				

RETH Type E17 SMEC-101

1.	new no.	LNRRI';	3DT'				-45 V	SS4-601
		13	14				1,5	J1-2
2.	internal	LNR99';	11DT';	E2;	LNRHO-9'			SMEC-114
		15	16	17	19			
3.	new no.	LNRRI';	6DT';	LNRHO-9';	E2			
		10	11	12	9			

Fig. 4-6

AO' Type E1 SMEC-101

1.	Internal	LNR99'; 13	14DT' 14					
2.	new no.	LNRRI'; 11	7DT' 12					

LNR99 Type E9 SMEC-101

1.		LNRT8'; 8	LNRT4'; 9	LNRU8'; 10	LNRU4'; 11	GO' 12		
2.		MCR2 13						

LNRRI' Type E9 SMEC-101

1.	Call 3010	βHO'; 8	βT11'; 9	βU10'; 10	βout 11			
2.	SS4	MCR4; 13	3'; 14	2; 15	1NT' 16	-45 V	V3-3 20	

LNRRI'A Type E9 SMEC-101

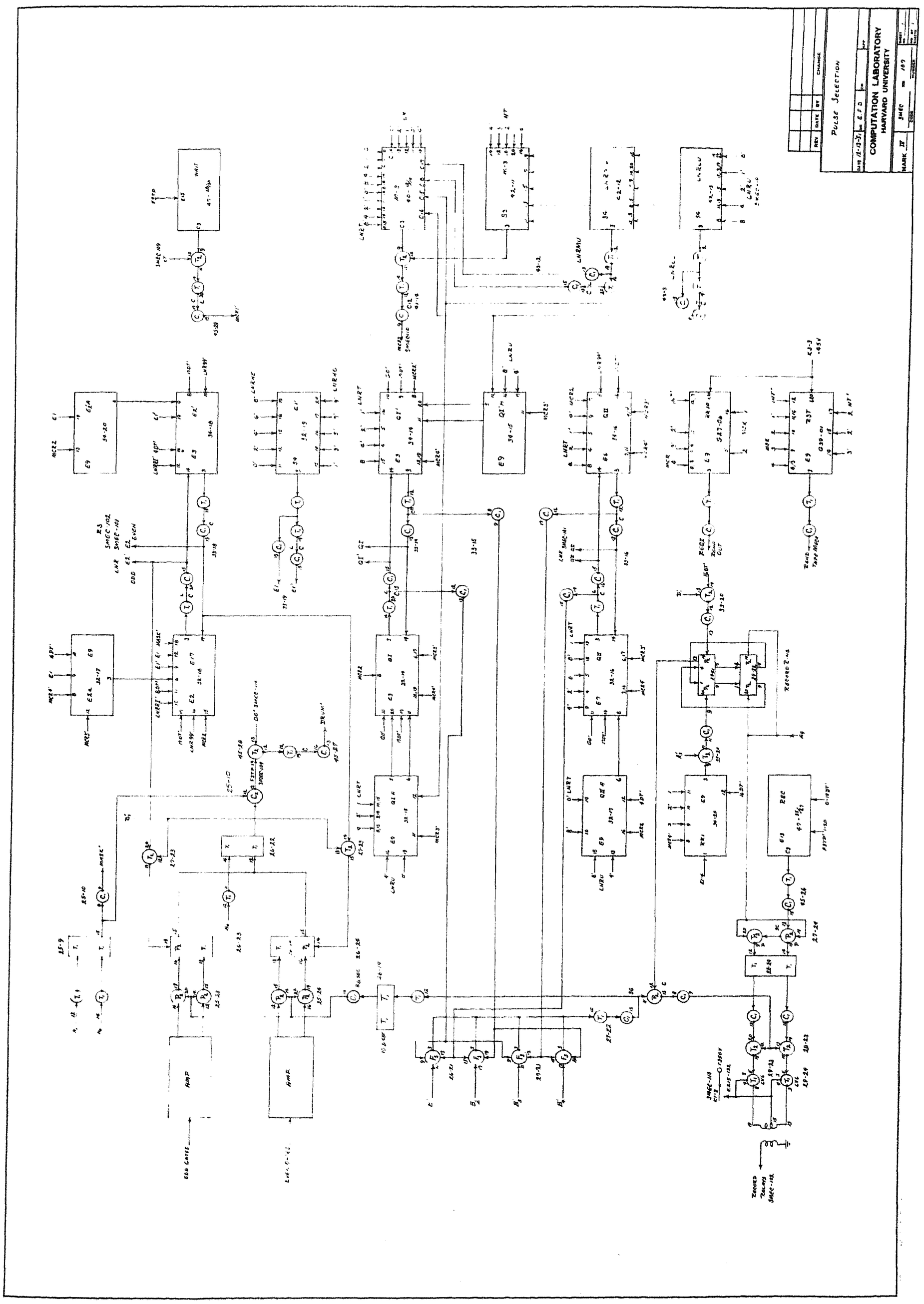
3.	SPEC line	MCR4; 8	3; 9	1'; 10	2NT' 11	-45 V	M4-3 1	
4.	Read-Run-Rec.	MCR4; 13	3'; 14	2'; 15	1'; 16	1NT' 17	-45 V 20	K3-3

Fig. 4-7

		1234						2987
DT:		1	2	3	4	5	6	7
LNRU	8'	0	0	1	1	1	1	1
	4'	1	0	0	0	0	0	0
	2'	0	0	1	1	1	1	1
	1'	0	0	0	0	0	0	0
	0'	1	0	0	0	0	0	0
LNRT	8'	1	0	0	1	1	1	1
	4'	0	0	0	0	0	0	0
	2'	0	0	0	0	0	0	0
	1'	1	0	0	0	0	0	0
	0'	0	0	0	1	1	1	1
LNRHO	9'	0	0	0	0	1	1	1
	7'	0	0	0	0	0	0	0
	5'	0	0	0	0	0	0	0
	3'	1	1	0	0	0	0	0
	1'	0	0	0	0	0	0	0
LNRHE	8'	0	0	0	0	0	0	0
	6'	0	0	0	0	0	0	0
	4'	0	0	0	0	0	0	0
	2'	1	1	0	0	0	0	0
	0'	0	0	0	0	0	0	1
LNRTHO	8'	0	0	0	0	0	0	0
	4'	0	0	0	0	0	0	0
	2'	0	0	0	0	0	1	1
	1'	1	1	0	0	0	0	0
	0'	1	1	0	0	0	1	1
LNRTHE	8'	0	0	0	0	0	0	1
	4'	0	0	0	0	0	0	0
	2'	0	0	0	0	1	0	0
	1'	1	1	1	0	0	0	1
	0'	1	1	1	0	0	1	0

Read-in to LNR

Fig. 4-8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COMPUTATION LABORATORY
HARVARD UNIVERSITY
MARK IV

Fig. 4-9

QII'	QI'	Quadrant	
1	1	I	0-24
1	0	II	25-49
0	1	III	50-74
0	0	IV	75-99

a) Quadrant

Sequence Gates in Control	E2'
odd	0
even	1

b) Odd-Even Selection

Note: 1 = low primed output
0 = high primed output

Fig. 4-10

DRUMLU Type S4 SMEC-101

1.	0-4	P*0'; 11	QI' 13	
2.	10-14	P*2'; 15	QI' 16	
3.	20-24	P*4'; 19	QI' 20	
4.	30-34	P*1'; 12	QI 14	
5.	40-44	P*3'; 18	QI 17	

Fig. 4-11

LNRU-2' Type E3 SMEC-101

1.	Hold	2'; 14	R 13		
2.	new no.	FIB2'; 10	LNRRI'; 9	2DT' 8	
3.	internal (7 2)	2NT'; 18	GO'; 19	16DT' 20	
4.	internal (5)	ONT'; 15	DRUMLU; 16	GO'; 12	16DT' 17
5.	internal (6)	1NT'; 4	DRUMLU; 5	GO'; 12	16DT' 6

Fig. 4-12

LNRTHE-4' Type E6 SMEC-101

1.	Hold	LNRTHE-4' 14	RETH 13		
2.	new no.	FIB4'; 17	LNRRI'; 15	5DT' 16	
3.	Add one	AOE'; 8	LNRHO-9'; 9	LNRTHO-8'; 10	2 11
4.	Add one	LNRTHE-4'; 6	LNRTHO-0' 7		

Fig. 4-13

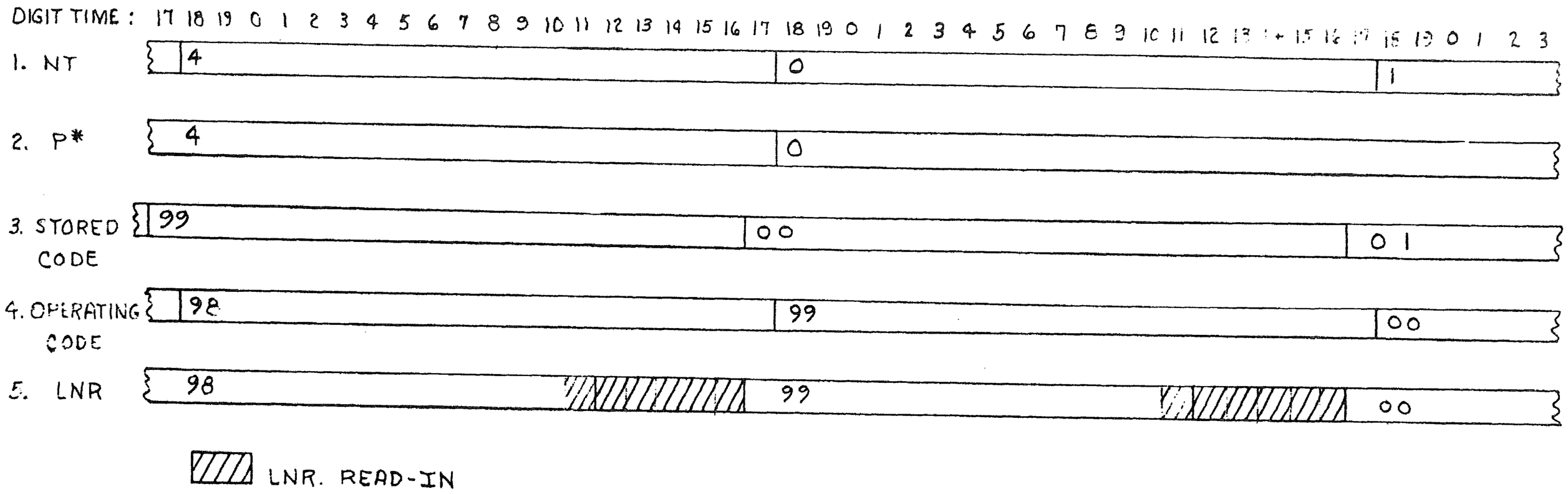
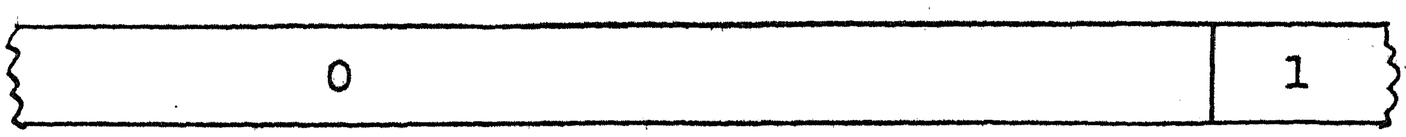


Fig. 4-14. Timing Diagram of Line Number Register Read-in



		DT: 11	12	13	14	15	16	17	18
LNRU	8'	1	1	1	1	0	0	0	0
	4'	1	1	1	1	0	1	1	1
	2'	0	0	0	0	0	0	0	0
	1'	0	0	0	0	0	1	1	1
	0'	0	0	0	0	0	0	0	0
LNRT	8'	1	1	1	1	0	0	0	0
	4'	1	1	1	1	0	1	1	1
	2'	0	0	0	0	0	0	0	0
	1'	0	0	0	0	0	1	1	1
	0'	0	0	0	0	0	0	0	0
LNRHE	8'	0	0	0	0	0	0	0	0
	6'	0	0	0	0	0	0	0	0
	4'	0	0	0	0	0	0	0	0
	2'	0	0	0	0	0	0	0	0
	0'	1	1	1	1	1	1	1	1
LNRHO	9'	1	0	0	0	0	0	0	0
	7'	0	0	0	0	0	0	0	0
	5'	0	0	0	0	0	0	0	0
	3'	0	0	0	0	0	0	0	0
	1'	0	0	0	1	1	1	1	1
LNRTHE	8'	0	0	0	0	0	0	0	0
	4'	1	1	1	1	1	1	1	1
	2'	0	0	0	0	0	0	0	0
	1'	1	1	1	1	1	1	1	1
	0'	0	0	0	0	0	0	0	0
LNRTHO	8'	1	0	0	0	0	0	0	0
	4'	1	0	0	1	1	1	1	1
	2'	0	0	0	0	0	0	0	0
	1'	0	0	0	1	1	1	1	1
	0'	0	0	0	0	0	0	0	0

Change in Line Number through Internal Cycling

Fig. 4-15

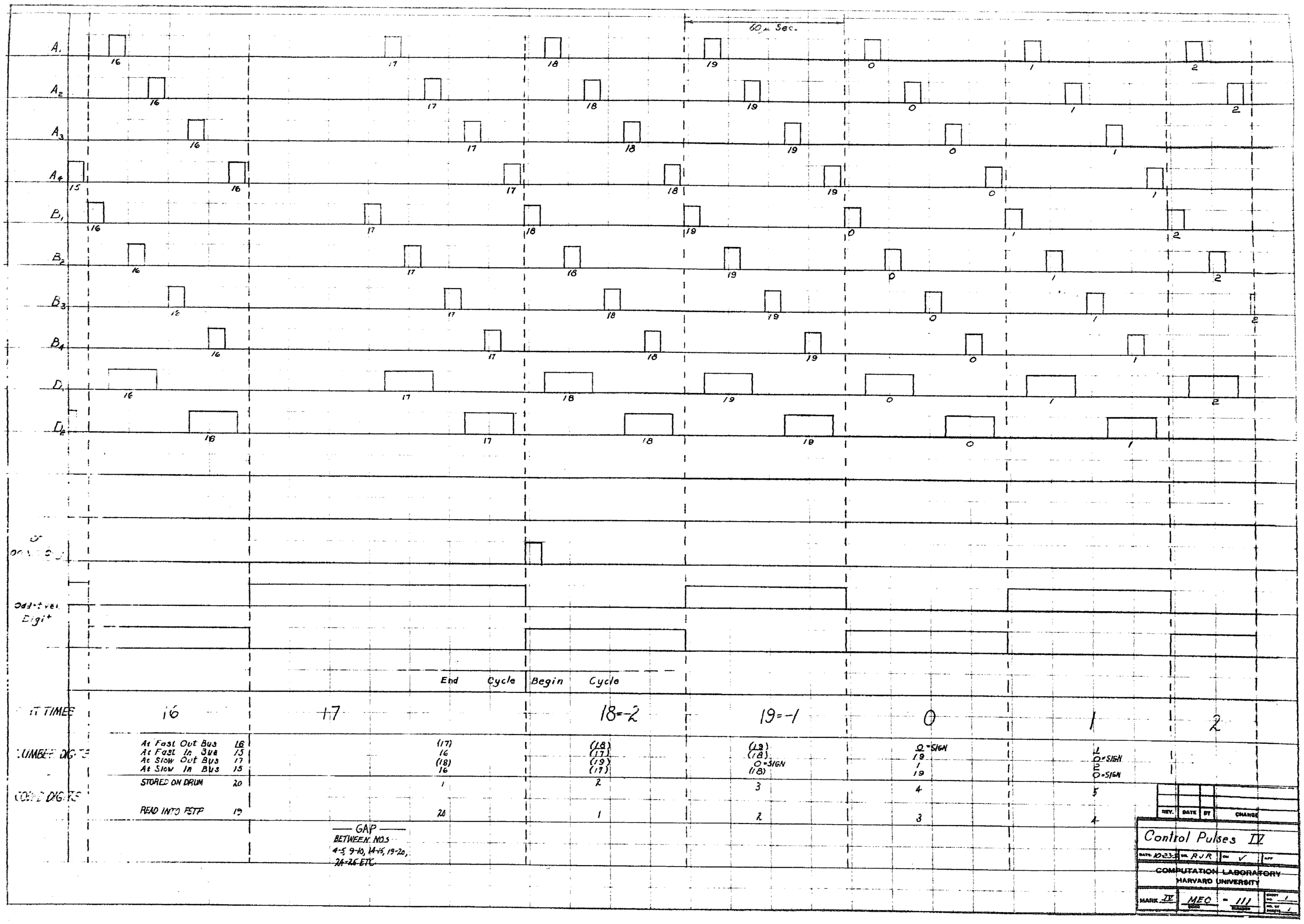

60 μ Sec.
A1
A2
A3
A4
B1
B2
B3
B4
D1
D2
Additive Digit
End Cycle
Begin Cycle
IT TIMEE
16
17
18=-2
19=-1
0
1
2
LUMBER DIGITS
At Fast Out Bus 16
At Fast In Bus 15
At Slow Out Bus 17
At Slow In Bus 15
STORED ON DRUM 20
READ INTO FSTP 19
(17) 16 (18) 16 1
(18) (17) (19) (17) 2
(19) (18) 0=SIGN (18) 3
0=SIGN 19 1 19 4
1 0=SIGN 0=SIGN 5
28 1 2 3 4
GAP
BETWEEN NOS
4-5, 9-10, 14-15, 19-20,
24-25 ETC.
REV. DATE BY CHANGE
Control Pulses IV
DATE 10-23-50 DR. R J R CH. ✓ APP.
COMPUTATION LABORATORY
HARVARD UNIVERSITY
MARK IV MEC - 111

Fig. 4-16

QI Type E3 SMEC-107

1.	Hold	QI 14				
2.	LNR 80-89 30-39 90-99	T8'; 15	T2; 16	MCR3'; 17	MCR4' 12	
3.	40-49	T4'; 4	TO'; 5	MCR3'; 6	MCR4' 12	
4.	25-29 75-79	QIA (5); 20	MCR4' 19			
5.	Change over 24,74	QIA (6); 11	17DT'; 9	GO'; 10	MCR2 8	

QIA Type E9 SMEC-107

4.	Output 5	T4; 8	T2'; 9	T1; 10	MCR3'; 11	LNRLU 12
5.	Output 6	T4; 13	T2'; 14	T1; 15	U4'; 16	UO' 17

Connect QIA (5) to QI (20)
" " (6) " " (11)

Fig. 4-17 (cont. on next page)

QI' Type E3 SMEC-107

1.	Hold	QI' 14				
2.	LNR 00-19	T8; 15	T1'; 16	MCR3'; 17	MCR4' 12	
3.	50-59	T4'; 4	T2'; 5	MCR3'; 6	MCR4' 12	
4.	20-24 70-74	QI'A (5); 20	MCR4' 19			
5.	Change over 49,99	QI'A (6); 11	17DT'; 9	GO'; 10	MCR2 8	

QI'A Type E9 SMEC-107

4.	Output 5	T4; 8	T2'; 9	T1; 10	MCR3'; 11	LNRLU' 12
5.	Output 6	T4'; 13	T2; 14	T1; 15	U8'; 16	U4' 17

Connect QI'A (5) to QI' (20)
" " (6) " " (11)

Fig. 4-17 (concluded)

QII Type E7 SMEC-107

1.	Hold	QII 14			
2.	LNR 50-69	T2'; 4	TO; 5	MCR3'; 6	MCR4' 7
3.	LNR 70-99	MCR4'; 16	T8'; 18	T1; 19	MCR3' 17
4.	Change over	QIIA (6); 8	17DT'; 10	GO'; 11	T4' 9

QIIA Type E9 SMEC-107

4.	Output 6	TO'; 14	U8'; 15	U4'; 13	MCR2 16

Connect QIIA (6) to QII (8)

QII' Type E6 SMEC-107

1.	Hold	QII' 14			
2.	LNR 30-39 00-19	T2; 4	T1'; 5	MCR3'; 6	MCR4' 7
3.	LNR 10-29 40-49	T8; 8	TO'; 9	MCR3'; 10	MCR4' 11
4.	Change over 99	LNR99'; 15	17DT'; 16	MCR2 17	

Fig. 4-18

E1' Type S4 SMEC-107

1.	LNRHE-0'; 11	LNRHO-1' 13				
2.	LNRHE-2'; 12	LNRHO-3' 14				
3.	LNRHE-4'; 15	LNRHO-5' 16				
4.	LNRHE-6'; 18	LNRHO-7' 17				
5.	LNRHE-8'; 19	LNRHO-9' 20				

E2 Type E17 SMEC-107

1.	Hold	E2 14				
2.	LNR	LNRRI'; 10	2DT'; 11			-45 V SS4-601, J1-2 4
3.	Change over	LNR99'; 16	17DT'; 17	E1'; 19	MCR2; 15	MASK' 18

E2A Type E9

4.		MCR4'; 8	E1; 9	16DT'; 10	MCR3' 12	Join E2A(3), E2(6)

E2' Type E3 SMEC-107

1.	Hold	E2' 14				
2.		MCR4'; 20	E1'; 19	MCR3' 18		
3.	Change over	LNR99'; 10	17DT'; 8	E2'A(6); 9	MASK' 11	
4.	LNR	LNRRI'; 12	4DT'; 6	FIB8; 7	FIB1'; 4	FIB0 5
5.	LNR	LNRRI'; 12	4DT'; 16	FIB1; 15	FIB0' 17	

E2'A Type E9

3.	Change over	MCR2; 13	E1 14		Join E2'(9), E2'A(6)

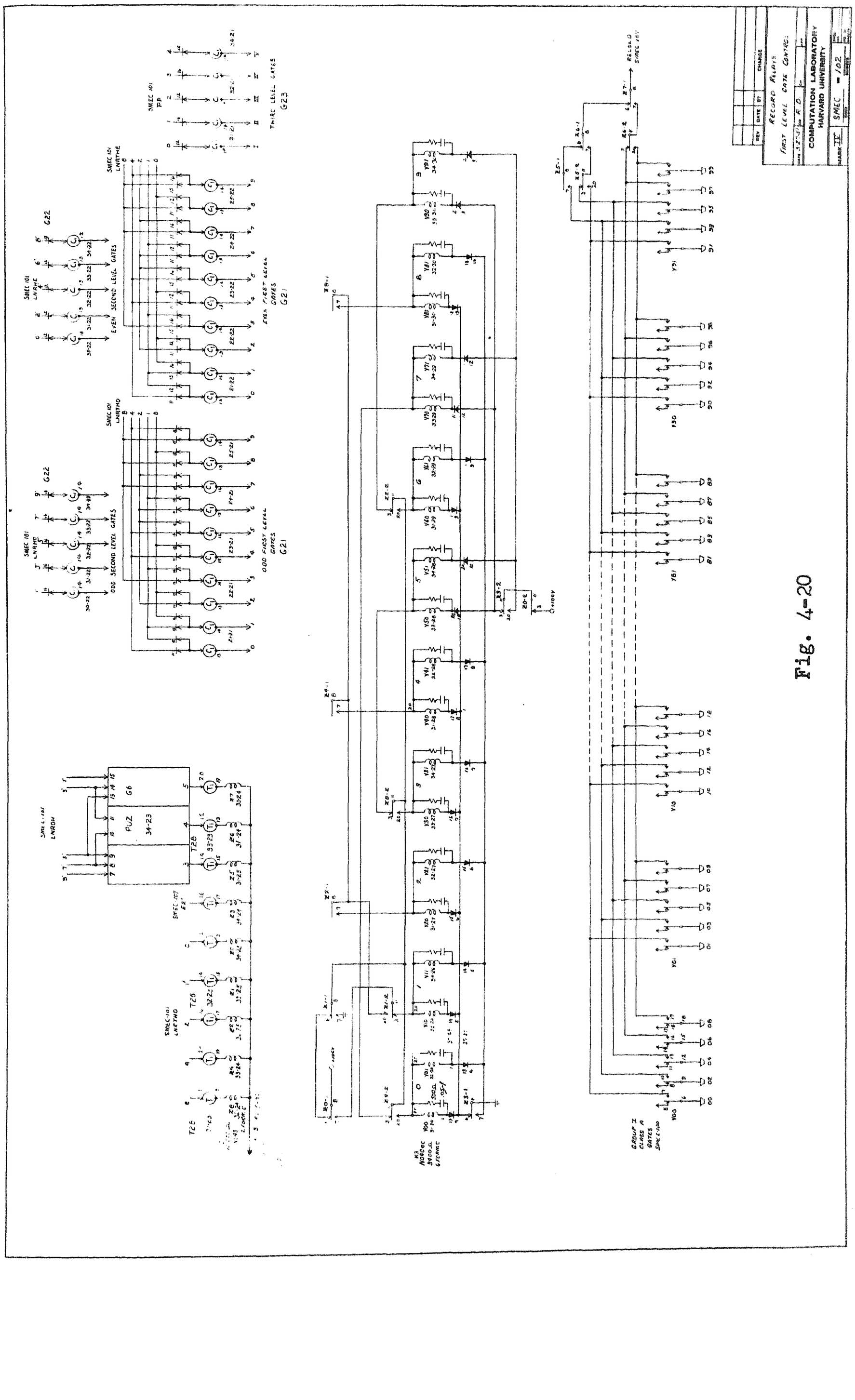

COMPUTATION LABORATORY
HARVARD UNIVERSITY
MARK III SMEC - 102
RECORD RELAYS
FIRST LEVEL GATE CONTROL
THIRD LEVEL GATES
G23
SECOND LEVEL GATES
G22
FIRST LEVEL GATES
G21
G6
T26
PU2
34-23
RELOAD
SMEC 101
LNRTHD
LNRTHE
PP
YB0
YB1
Y00
Y01
Y10
Y11
Y20
Y21
Y30
Y31
Y40
Y41
Y50
Y51
Y60
Y61
Y70
Y71
Y80
Y81
Y90
Y91
130
K3
NOVEC
3400 A
GROMC
GROUP II
CLASS A
GATES
SMEC 100

Fig. 4-20

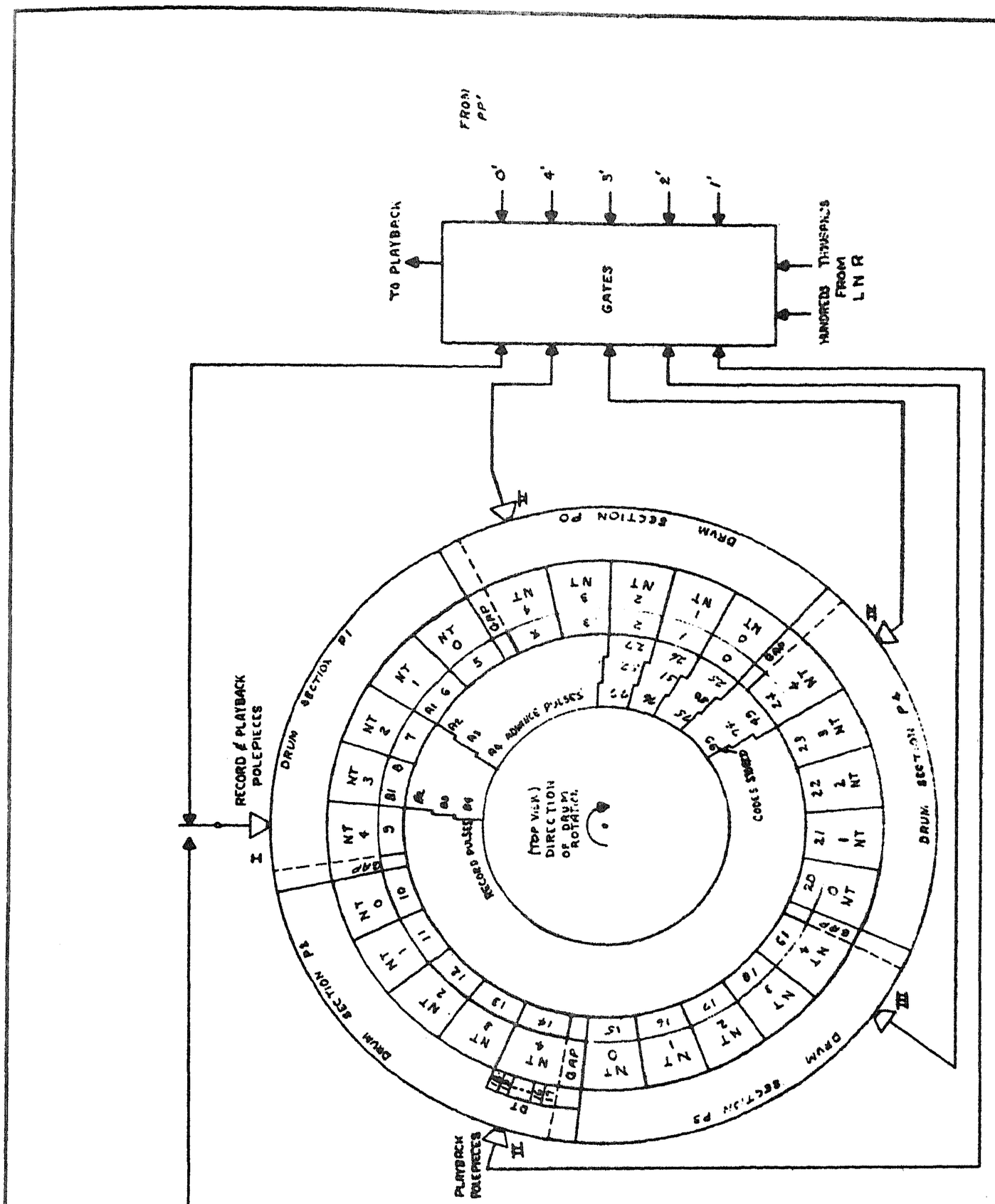


Fig. 4-21. Subdivision of Drum Circumference

LNRLU Type S4 SMEC-107

1.	0	LNRU4'; 11	LNRU1' 13
2.	1	LNRU1'; 12	LNRU0' 14
3.	2	LNRU2'; 15	LNRU0' 16
4.	3	LNRU8'; 18	LNRU1' 17
5.	4	LNRU4'; 19	LNRU0' 20

Fig. 4-22

LNRMU Type S4 SMEC-107

1.	LNR 7	U2'; 11	U8' 13
2.	" 3	U8'; 12	U1' 14
3.	" 4	U4'; 15	U0' 16
4.	" 5	U4'; 18	U2' 17
5.	" 6	U2'; 19	U1' 20

Fig. 4-23

m-3 Type S3 SMEC-107

1.	LNRO	U4'; 13	U1'; 17	2NT' 10
2.	" 5	U4'; 13	U2'; 15	2NT' 10
3.	" 1	U1'; 17	UO'; 19	3NT' 12
4.	" 6	U2'; 15	U1'; 17	3NT' 12
5.	" 2	U2'; 15	UO'; 19	4NT' 14
6.	" 7	U8'; 11	U2'; 15	4NT' 14
7.	" 3	U8'; 11	U1'; 17	ONT' 16
8.	" 8	U8'; 11	UO'; 19	ONT' 16
9.	" 4	U4'; 13	UO'; 19	1NT' 20
10.	" 9	U8'; 11	U4'; 13	1NT' 20

Fig. 4-24

M-3 Type E19 SMEC-107

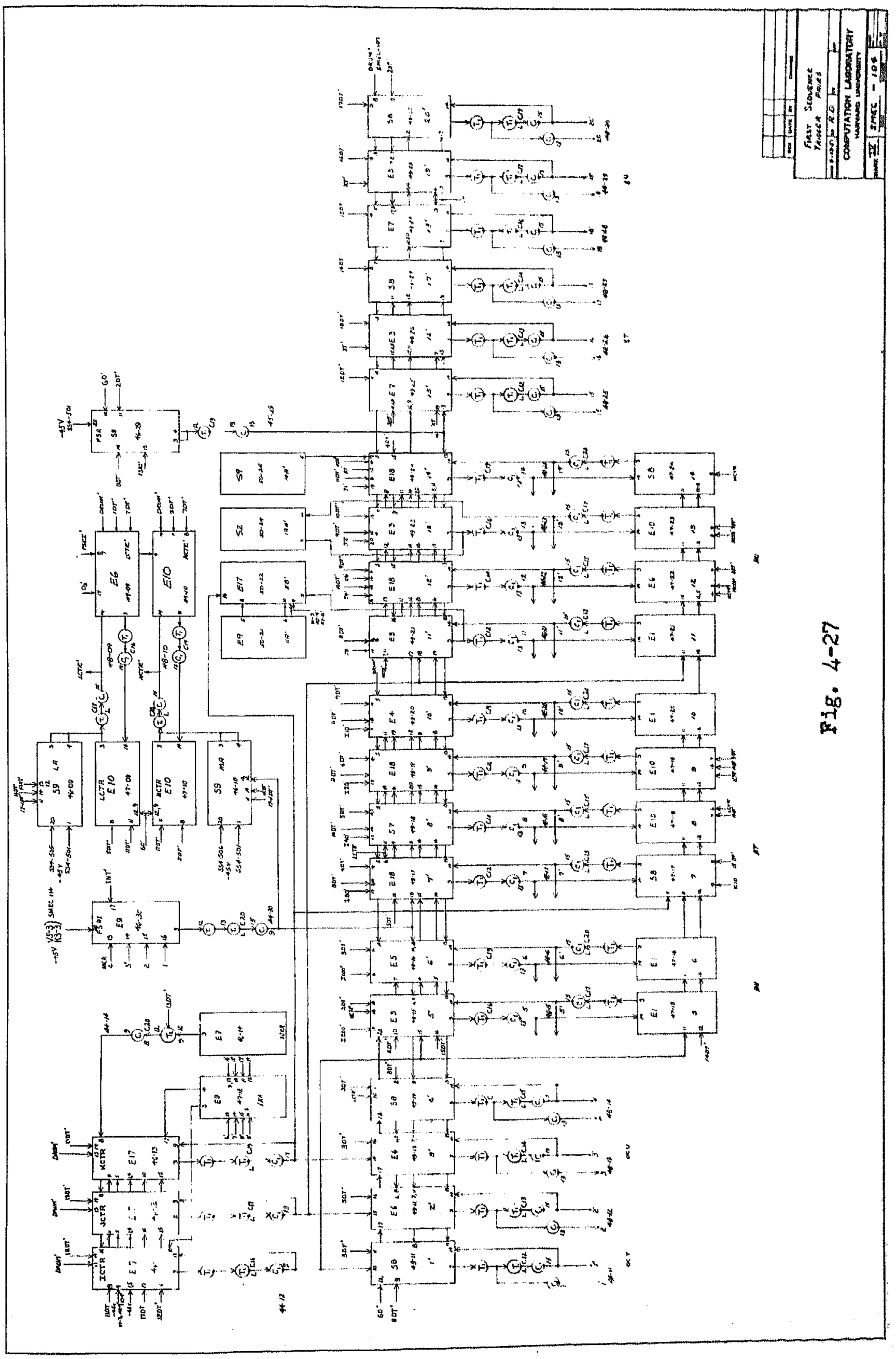
1.	98-99 48-49	LNRT4'; A14	LNRT2; B12	LNRT1; B11	LNRLU; C15	LNRMU; C17	P*4' C10
2.	00-02 50-52	LNRT8; B18	LNRT4'; A14	LNRT0; B10	LNRLU'; C16	LNRMU; C17	P*4' C10
3.	23-27 73-77	LNRT4; B14	LNRT2'; A12	LNRT1; B11	LNRMU'; C18	P*4' C10	
4.	28-29 78-79	LNRT4; B14	LNRT2'; A12	LNRT1; B11	LNRLU; C15	LNRMU; C17	P*0' C11
5.	30-32 80-82	LNRT8'; A18	LNRT4; B14	LNRT2; B12	LNRLU'; C16	LNRMU; C17	P*0' C11
6.	03-07 53-57	LNRT8; B18	LNRT4'; A14	LNRT0; B10	LNRMU'; C18	P*0' C11	
7.	08-09 58-59	LNRT8; B18	LNRT4'; A14	LNRT0; B10	LNRLU; C15	LNRMU; C17	P*1' C12
8.	10-12 60-62	LNRT8; B18	LNRT4; B14	LNRT1'; A11	LNRLU'; C16	LNRMU; C17	P*1' C12
9.	33-37 83-87	LNRT8'; A18	LNRT4; B14	LNRT2; B12	LNRMU'; C18	P*1' C12	
10.	38-39 88-89	LNRT8'; A18	LNRT4; B14	LNRT2; B12	LNRLU; C15	LNRMU; C17	P*2' C13
11.	40-42 90-92	LNRT4'; A14	LNRT2; B12	LNRT1; B11	LNRLU'; C16	LNRMU; C17	P*2' C13
12.	13-17 63-67	LNRT8; B18	LNRT4; B14	LNRT1'; A11	LNRMU'; C18	P*2' C13	
13.	18-19 68-69	LNRT8; B18	LNRT4; B14	LNRT1'; A11	LNRLU; C15	LNRMU; C17	P*3' C14
14.	20-22 70-72	LNRT4; B14	LNRT2'; A12	LNRT1; B11	LNRLU'; C16	LNRMU; C17	P*3' C14
15.	43-47 93-97	LNRT4'; A14	LNRT2; B12	LNRT1; B11	LNRMU'; C18	P*3' C14	

Fig. 4-25

PP2' Type E10

1.	Hold 1	PP2'; 10	2DT; 11	9DT 12			
2.	Hold 2	PP2'; 14	MCR3 13				-45 1
3.	Try	MCR4'; 6	3'; 7	2; 8	8DT' 9		

Fig. 4-26


FIRST SEQUENCE TRACER PROBE
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SMEC - 104

Fig. 4-27

α tens	FSTP1'
0	1
1	0

α units γ tens γ units	FSTP 2' 3' 4' 15' 16' 17' 18' 19' 20'
0	1 1 1
1	0 0 1
2	0 1 0
3	1 0 1
4	1 0 0
5	1 1 0
6	0 1 1
7	0 0 0

β hundreds	FSTP 5' 6'
0	1 1
1	1 0
2	0 1
3	0 0

β tens β units	FSTP 7' 8' 9' 10' 11' 12' 13' 14'
0	0 1 0 1
1	0 0 0 1
2	0 0 1 0
3	1 0 0 1
4	0 1 0 0
5	0 1 1 0
6	0 0 1 1
7	1 0 1 0
8	1 0 0 0
9	1 1 0 0
10	1 1 1 1
11	0 1 1 1
12	1 0 1 1
13	1 1 0 1
14	1 1 1 0
15	0 0 0 0

β thousands	β tens	β units
0	1st group	1st group
1	" "	2nd "
2	2nd "	1st "
3	" "	2nd "
	LCTR'	MCTR'
0	0	0
1	0	1
2	1	0
3	1	1

Fig. 4-28

DT:	7	8	9	10	11	
FSTP						
7 (11)	0	1	1	1	1	
8 (12)	1	1	1	1	1	0 ⟶ 10
9 (13)	0	0	1	1	1	
10 (14)	1	1	1	1	1	
7 (11)	0	0	0	0	0	
8 (12)	0	0	0	1	1	1 ⟶ 11
9 (13)	0	0	1	1	1	
10 (14)	1	1	1	1	1	
7 (11)	0	1	1	1	1	
8 (12)	0	0	0	0	0	2 ⟶ 12
9 (13)	1	1	1	1	1	
10 (14)	0	0	0	0	1	
7 (11)	1	1	1	1	1	
8 (12)	0	0	0	1	1	3 ⟶ 13
9 (13)	0	0	0	0	0	
10 (14)	1	1	1	1	1	
7 (11)	0	1	1	1	1	
8 (12)	1	1	1	1	1	4 ⟶ 14
9 (13)	0	0	1	1	1	
10 (14)	0	0	0	0	0	
7 (11)	0	0	0	0	0	
8 (12)	1	1	1	0	0	5 ⟶ 15
9 (13)	1	1	0	0	0	
10 (14)	0	0	0	0	0	

Fig. 4-29

SMEC-104

FSTP-11	Type E1						
1. Hold	11 14						
2. J reset	JCTR'; 11	14DT' 12					

SMEC-104

FSTP-11'	Type E3						
1. Hold	11'; 14	FSR 13					
2. J in	JCTR'; 18	15DT'; 19	J8' 20				
3. Bus	FIB8'; 15	4DT'; 16	FSRI' 17				
4. "	MCTR'; 11	8DT'; 8	FSTP-12'; 9	FSTP-13 10			
5. "	MCTR'; 7	8DT'; 4	FSTP-12; 5	FSTP-13' 6			

FSTP-11'A	Type E9						
6. CC in	CC'; 8	17DT'; 9	FSTP-5'; 10	6'; 11	7 12		
6. CC in	FSTP-8'; 13	9'; 14	10'; 15	12'; 16	14' 17		

FSTP-11'B	Type E17						
6. CC in	11'A(5); 8	FSTP13'; 9	11'A(6) 10		-45 V 4	X1-3 M2-4' K1-4'	
7. Drum	Drum'; 13	8DT' 14					
8. K in	KCTR'; 16	15DT'; 17	K8' 15				

Connect 11' (3), 11'B(3)
" 11'A(5), 11'B(8)
" 11'A(6), 11'B(10)

Fig. 4-30

FSTP-12 Type E6 SMEC-104

1. Hold	12 14			
2. Bus	MCTR'; 8	10DT'; 9	FSTP-13; 10	FSTP-14 11
3. J reset	JCTR'; 15	14DT' 16		
4. K reset	KCTR'; 4	14DT' 5		

FSTP-12' Type E18 SMEC-104

1. Hold	12'; 14	FSR 13		
2. Drum	Drum'; 5	9DT' 4		
3. Bus	FIB4'; 17	4DT'; 15	FSRI' 16	
4. "	MCTR'; 19	10DT'; 18	FSTP14' 20	
5. J in	JCTR'; 8	15DT'; 6	J4' 7	
6. K in	KCTR'; 11	15DT'; 6	K4' 10	

Fig. 4-31

FSTP-13 Type E10 SMEC-104

1.	Hold	13 14			
2.	Bus	MCTR'; 8	9DT'; 9	FSTP-11; 6	FSTP-12' 7
3.	J reset	JCTR'; 11	14DT' 12		

FSTP-13' Type E3 SMEC-104

1.	Drum	Drum'; 14	10DT' 13		
2.	Bus	FIB2'; 8	4DT'; 9	FSRI' 10	
3.	"	MCTR'; 12	9DT'; 15	FSTP-11'; 16	FSTP-12' 17
4.	"	MCTR'; 12	9DT'; 4	FSTP-11; 5	FSTP-14' 6
5.	J in	JCTR'; 18	15DT'; 19	J2' 20	

FSTP-13'A Type S2 SMEC-104

1.	Hold	13'; 14	FSR 13		Connect 13'(3), 13'A(3)
2.	K in	KCTR'; 10	15DT'; 11	K2' 12	

Fig. 4-32

FSTP-14	Type S8			SMEC-104
1. Hold	14 14			
2. J reset	JCTR'; 11	14DT' 12		
3. K reset	KCTR'; 8	14DT' 9		

FSTP-14'	Type E18			SMEC-104
1. Hold	14'; 14	FSR 13		
2. Drum	Drum'; 5	11DT' 4		
3. Bus	FIB1'; 17	4DT'; 15	FSRI' 16	
4. "	MCTR'; 8	11DT'; 9	FSTP-14'A(5) 7	
5. J in	JCTR'; 20	15DT'; 18	J1' 19	
6. K in	KCTR'; 11	15DT'; 10	K1' 12	

FSTP-14'A	Type S9		
4. Bus	FSTP-12; 10	FSTP-13' 11	

Fig. 4-33

FSR Type S9 SMEC-104

1.	GO'; 12	2DT' 11				
2.	FSRI'; 13	ODT' 14				-45 V SS4-501 20

FSRI Type E9 SMEC-104

1.	MCR-4; 13	3' 14	2; 15	1; 16	1NT' 17	-45 V { K3-3 V5-3 SMEC-114 20

Fig. 4-34

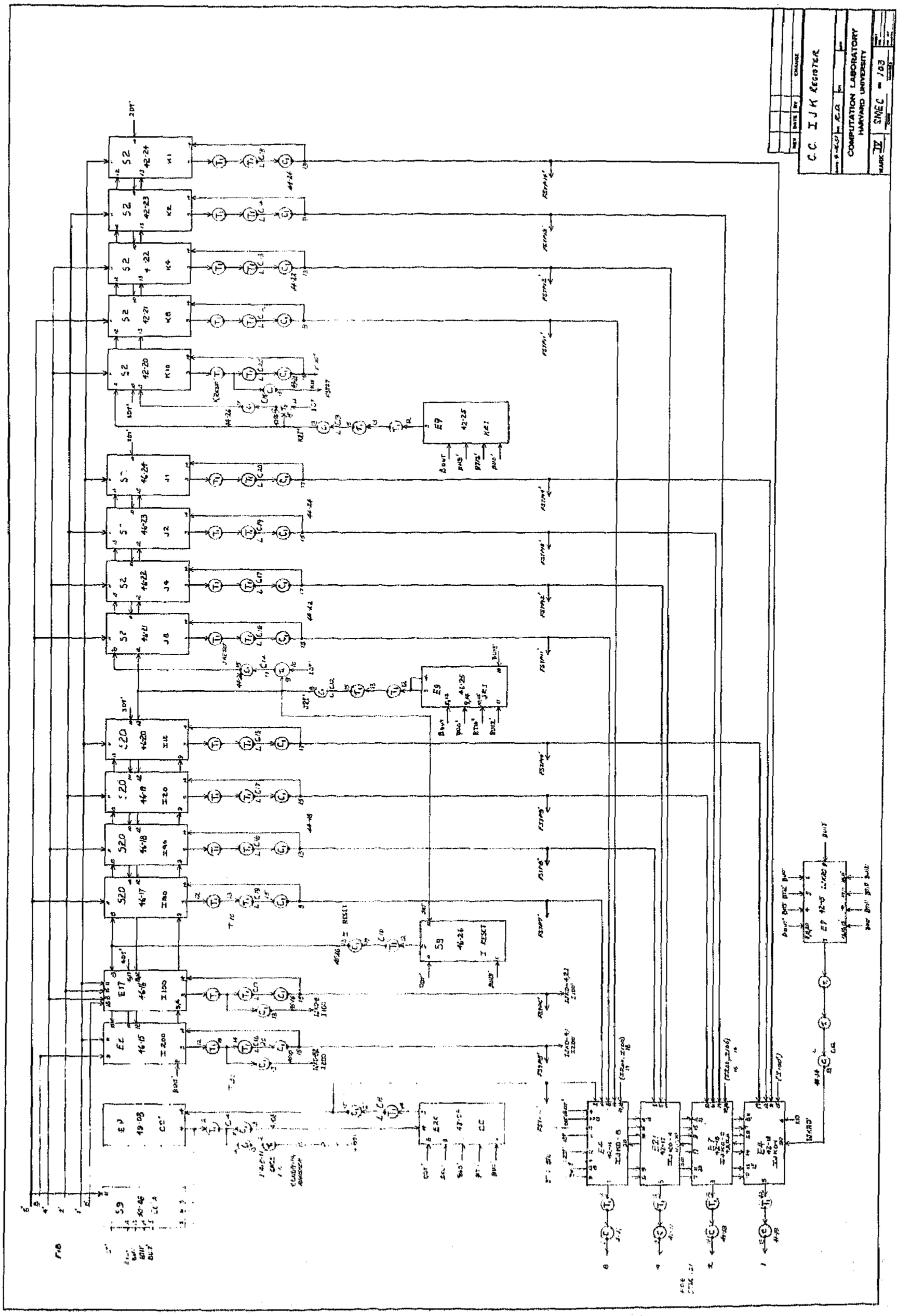

C.C. IJK REGISTER
COMPUTATION LABORATORY
HARVARD UNIVERSITY
SIZE
SNEC - 103

Fig. 4-35

ICTR	Type E17				SMEC-104
1. Hold	ICTR'; 16	IJKR; 17	17DT; 18	11DT 19	
2. Drum	Drum'; 13	18DT' 14			
3. I Control	IKA(6); 10	12DT' 11			-45 V, X1-3,M2-4',K1-4' 4

IKA	Type E9					SMEC-104
Output 6	FSTP-6'; 13	7'; 14	8'; 15	9'; 16	10' 17	

Connect IKA (6) to ICTR (10)

Fig. 4-36

JCTR	Type E17					SMEC-104
1. Hold	JCTR'; 9	IJKR; 8	17DT; 10	11DT 11		
2. Drum	Drum'; 13	19DT' 14				
3. J Control	FSTP:11' 19	12'; 18	13'; 17	14'; 16	12DT' 15	-45 V X1-3, M2-4', K1-4' 5

Fig. 4-37

KCTR	Type E17					SMEC-104
1. Hold	KCTR'; 9	IJKR; 8	17DT; 10	11DT 11		
2. Drum	Drum'; 13	ODT' 14				
3. K control	FSTP:5; 19	6; 16	8'; 18	12DT'; 15	IKA(5) 17	-45 V 5 X1-3, M2-4', K1-4'

IKA	Type E9					SMEC-104
Output 5	FSTP:9'; 8	10'; 9	12'; 10	13; 11	14' 12	

Connect IKA (5) to KCTR (17)

Fig. 4-38

IJKR	Type E7				SMEC-104
1. I correction	FSTP:11'; 4	12 ; 5	13'; 6	14' 7	
2. I "	FSTP:11'; 8	12'; 9	13; 10	14' 11	
3. J "	FSTP:7; 12	8'; 13	9'; 14	10' 15	
4. J "	FSTP:5; 16	6'; 17	7'; 18	8' 19	

Fig. 4-39

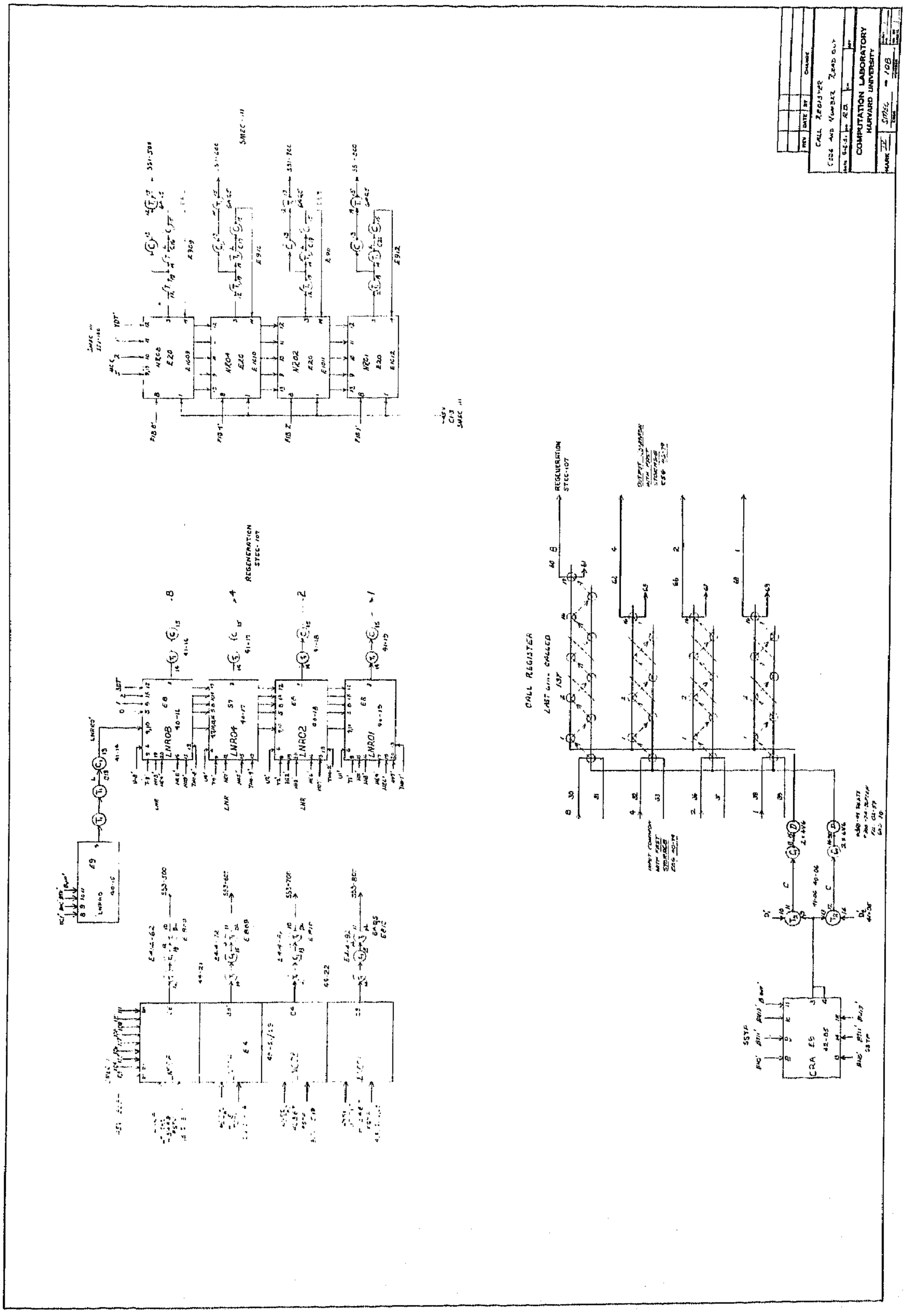

CALL REGISTER
COMPUTATION LABORATORY
HARVARD UNIVERSITY
REGENERATION
STEC-107
REGENERATION
STEC-107
CALL REGISTER
LAST WORD CHANGED

Fig. 4-40

J8	Type S2				SMEC-103
1. Hold	J Reset; 13	J8' 14			
2. Bus	FIB8'; 11	2DT'; 10	JRI' 12		

I20	Type S20				SMEC-103
1. Hold	I Reset; 13	I20' 14			
2. Bus	FIB2'; 11	3DT'; 10	JRI'; 12	βU13' 9	

I100	Type E17					SMEC-103
1. Hold	I Reset; 13	I100' 14				
2. Bus	FIB4'; 8	FIB1'; 11	4DT'; 10	JRI'; 12	βU13' 9	
3.	FIB2'; 15	FIB0'; 18	4DT'; 17	JRI'; 19	βU13' 16	

I200	Type E2				SMEC-103
1. Hold	I Reset; 13	I200' 14			
2. Bus	FIB8; 9	FIB1'; 11	4DT'; 10	JRI'; 12	βU13' 8

Fig. 4-41

I Reset	Type S9			SMEC-103
1. β3003 in	0DT'; 10	JRI'; 12	βU13' 11	

JRI	Type E9				SMEC-103
1. β3002 in	βout; 8	βH0'; 9	βT10'; 10	βU12' 11	
2. β3003 in	βout; 13	βH0'; 14	βT10'; 15	βU13' 16	

connect 3, 4

Fig. 4-42

IJKRO	Type E7				SMEC-103
1. K out (β2320)	βout'; 7	βH3'; 4	βT12'; 5	βU0' 6	
2. J out (β3002)	βout'; 20	βH0'; 16	βT10'; 17	βU12' 18	
3. IJ out (β3003)	βout'; 8	βH0'; 10	βT10'; 11	βU13' 9	
4. CC out (β3012)	βout'; 12	βH0'; 13	βT11'; 14	βU12' 15	

Fig. 4-43

CC Type E20 SMEC-103

1. Hold	CC 14					
2. Reset β3012	ODT'; 8	βout; 9	βHO'; 10	βT11'; 11	βU11' 12	

CC' Type E9 SMEC-103

1. Hold	CC' 14				

CC'A Type S9 SMEC-103

4. Bus 3012	1DT'; 10	FIB8'; 11	βout 12	Connect CC'A(5),CC'A(6). Connect CC'(6),CC'A(3).	
	βHO'; 13	βT11'; 14	βU11' 15		

Fig. 4-44

IJKO-8 Type E4 SMEC-103

1. CC	IJKRO'; 20	19DT'; 4	CC'; 5	βT11' 6	
2. I/J	IJKRO'; 20	ODT'; 7	J8'; 8	βT10' 9	
3. I/J	IJKRO'; 20	1DT'; 10	I80'; 11	βU13' 12	
4. I/J	IJKRO'; 20	2DT'; 16	I200; 17	I100; 18	βU13' 19
5. K	IJKRO'; 20	ODT'; 13	K8'; 14	βT12' 15	

Fig. 4-45

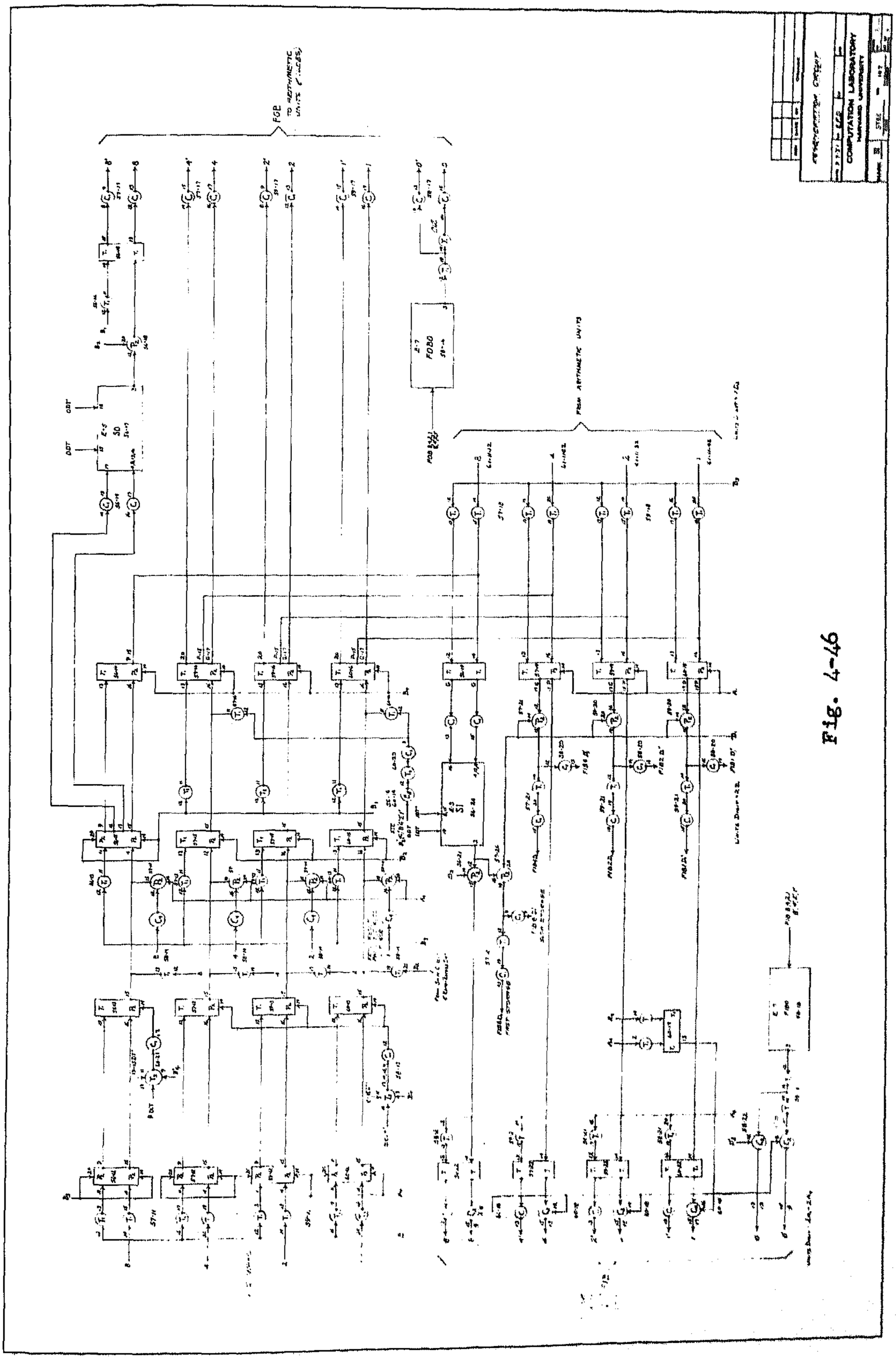


Fig. 4-46

CRA		Type E9				SMEC-108
1.	β3010	βHO'; 8	βT11'; 9	βU10'; 10	βout 11	
2.	β3013	βHO'; 13	βT11'; 14	βU13' 15		connect 3,4

Fig. 4-47

SSTP-α1'		Type E1				SMEC-115
1.	Hold	α1'; 14	SSTPR 13			
2.	FSTP	1'; 11	αCA' 12			

SSTP-βHO'		Type S2				SMEC-116
1.	Hold	SSTPR; 13	βHO' 14			
2.	FSTP	βCA'; 12	5'; 10	6' 11		

SSTP-βUO'		Type E2					SMEC-116
1.	Hold	SSTPR; 13	βUO' 14				
2.	FSTP	βCA'; 12	11; 8	12'; 9	13; 10	14' 11	

SSTP-γTO'		Type S20				SMEC-115
1.	Hold	γTO'; 14	SSTPR 13			
2.	FSTP	15'; 9	16'; 10	17'; 11	γCA' 12	

Fig. 4-48

CA		Type E17					SMEC-115
1.	Operate	MCR4; 15	MCR3'; 16	MCR2; 17	1NT'; 18	18DT' 19	-45 V X1-3 5
2.	Regular	GO'; 8	MCR2; 9	18DT' 10			-45 V M2-4' 4
3.	Repeat	18DT' 14					-45 V X4-3 1
CAA		Type E9					
4.	Button	MCR3'; 4	MCR2; 10	MCR1'; 12	2NT'; 11	18DT' 8	-45 V C1-3 1
				Join CAA(3), CA(6)			
βCAR		Type E17					SMEC-115
1.	XT	XT' 13					-45 V C1-3 4
2.	γ out	FSTP-1 8					
3.	γ out	FSTP-3; 15	FSTP-4 16				-45 V C1-3 5
γCAR		Type E9					SMEC-115
1.	XT	XT' 11					
2.	βout	FSTP-1' 17					-45 V C1-3 20
SSTPR		Type E9					SMEC-115
1.		18DT'; 8	D1' 9				

Fig. 4-49

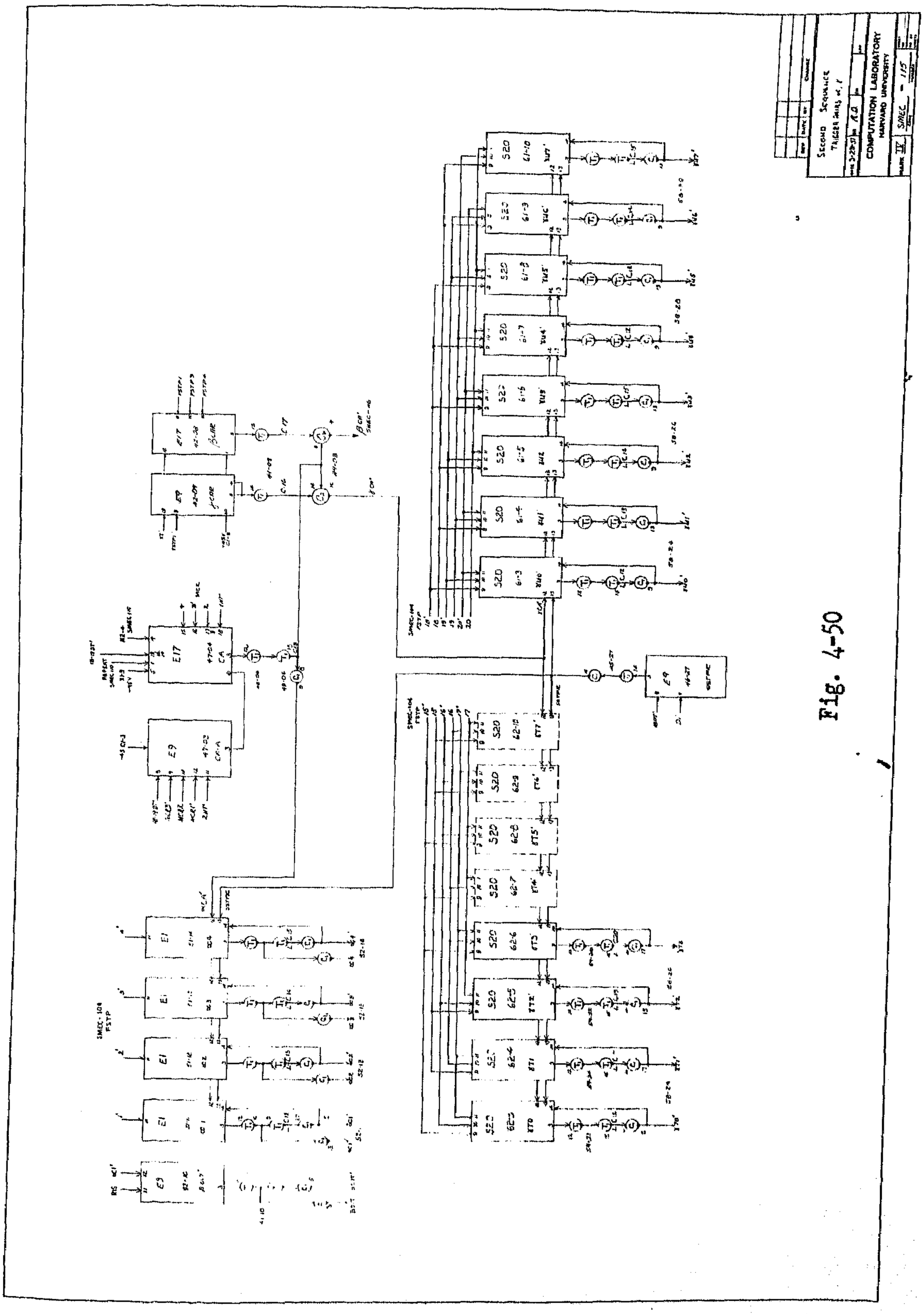

COMPUTATION LABORATORY
HARVARD UNIVERSITY
SECOND SEQUENCE
TRIGGER UNIT #1
MARK IV
SAGEC - 115
DATE 3-29-51
BY A.G.
CHANGE
S20
E17
E9
E1
E3
SMEC-104
FSTP

Fig. 4-50

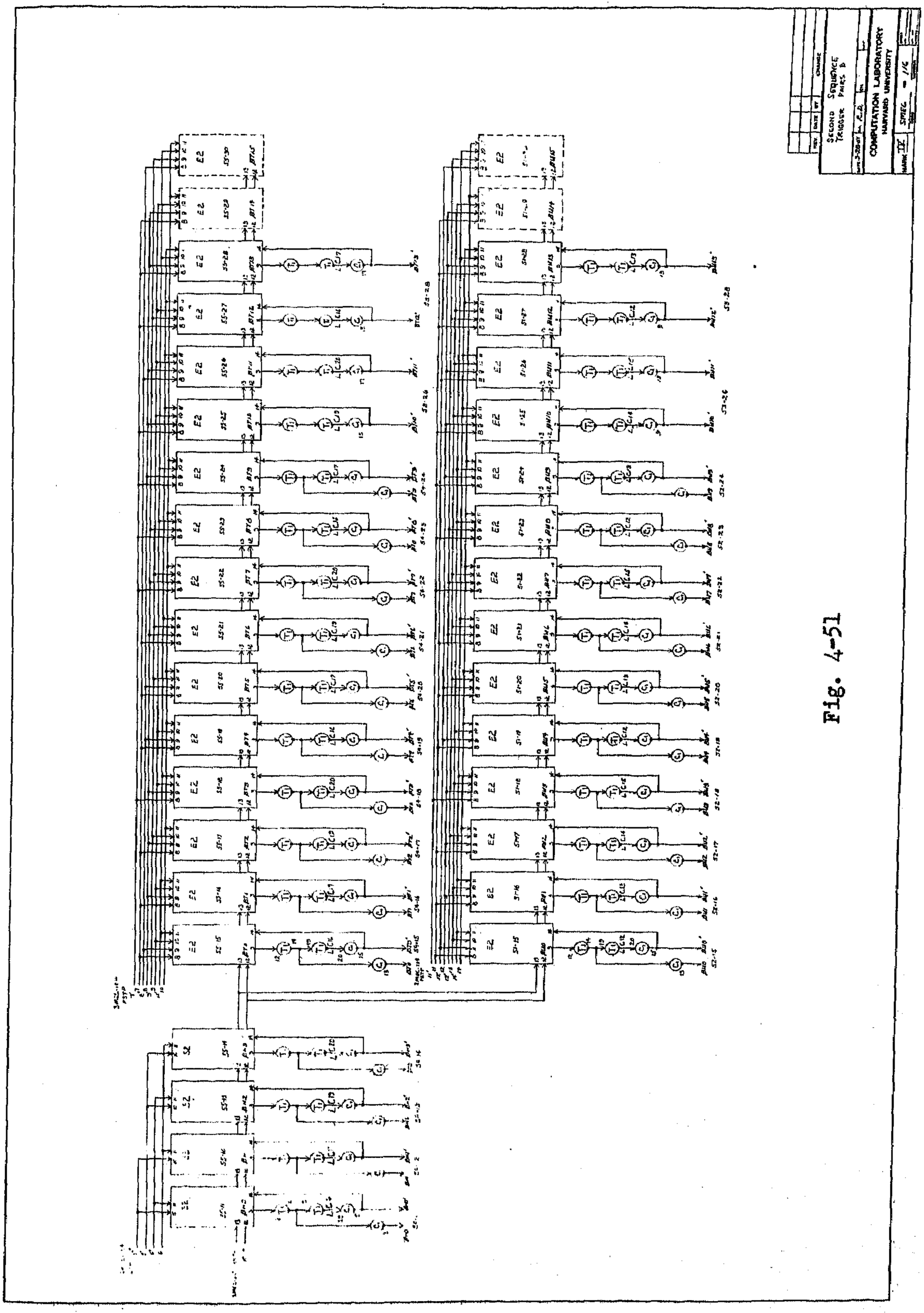

SECOND SEQUENCE TRIGGER PAIRS B
COMPUTATION LABORATORY
HARVARD UNIVERSITY

Fig. 4-51

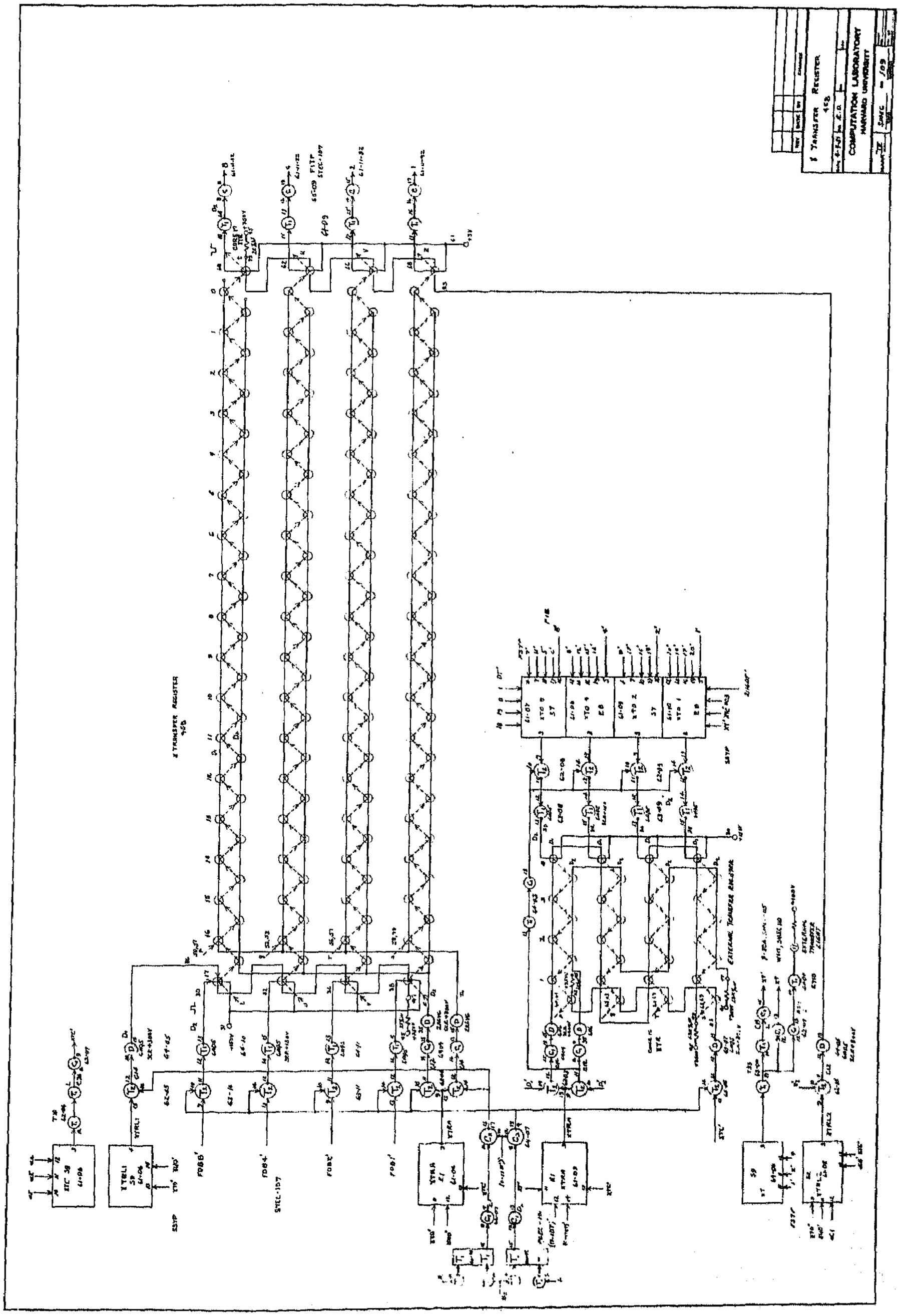


Fig. 4-52

XTRA	Type E1		SMEC-109
1. XT-1	XT'; 11	17-1DT' 12	
2. XT1-2	XTC'; 13	0-17DT' 14	

γTRA	Type E1		SMEC-109
1.	γTO'; 11	γUO' 12	
2. XT1-2	XTC' 13		

γTRL1	Type S9		SMEC-109
1.	γTC'; 13	γUC' 14	

γTRL2	Type S2			SMEC-109
1. Transfer Register Out	γTO'; 10	γUO'; 11	a1 12	
2. External Transfer with shift	XTC'; 13	SSTPa3' 14		

XT'	Type S9			SMEC-109
1. FSTP	1'; 10	2'; 11	4 12	

XTC'	Type S9			
1.	SSTPa1'; 10	a2'; 11	a4 12	

Fig. 4-53

XTO-8 Type S7 SMEC-109

1.		FSTP-7'; 4	1DT'; 5	XT' 6
2.		11'; 7	0DT'; 8	XT' 9
3.		5'; 10	19DT'; 11	XT' 12
4.		6'; 13	18DT'; 14	XT' 15
5.		FIB8'; 16	2-16DT'; 17	XTC' 18

XTO-4 Type E8 SMEC-109

1.		FSTP8'; 12	1DT'; 13	XT' 10
2.		12'; 14	0DT'; 15	XT' 10
3.		15'; 16	19DT'; 17	XT' 10
4.		18'; 19	18DT'; 20	XT' 10
5.		FIB4'; 5	2-16DT'; 6	XTC' 4
6.	XT1	XTC '; 4	2-16DT'; 7	03 8

Fig. 4-54

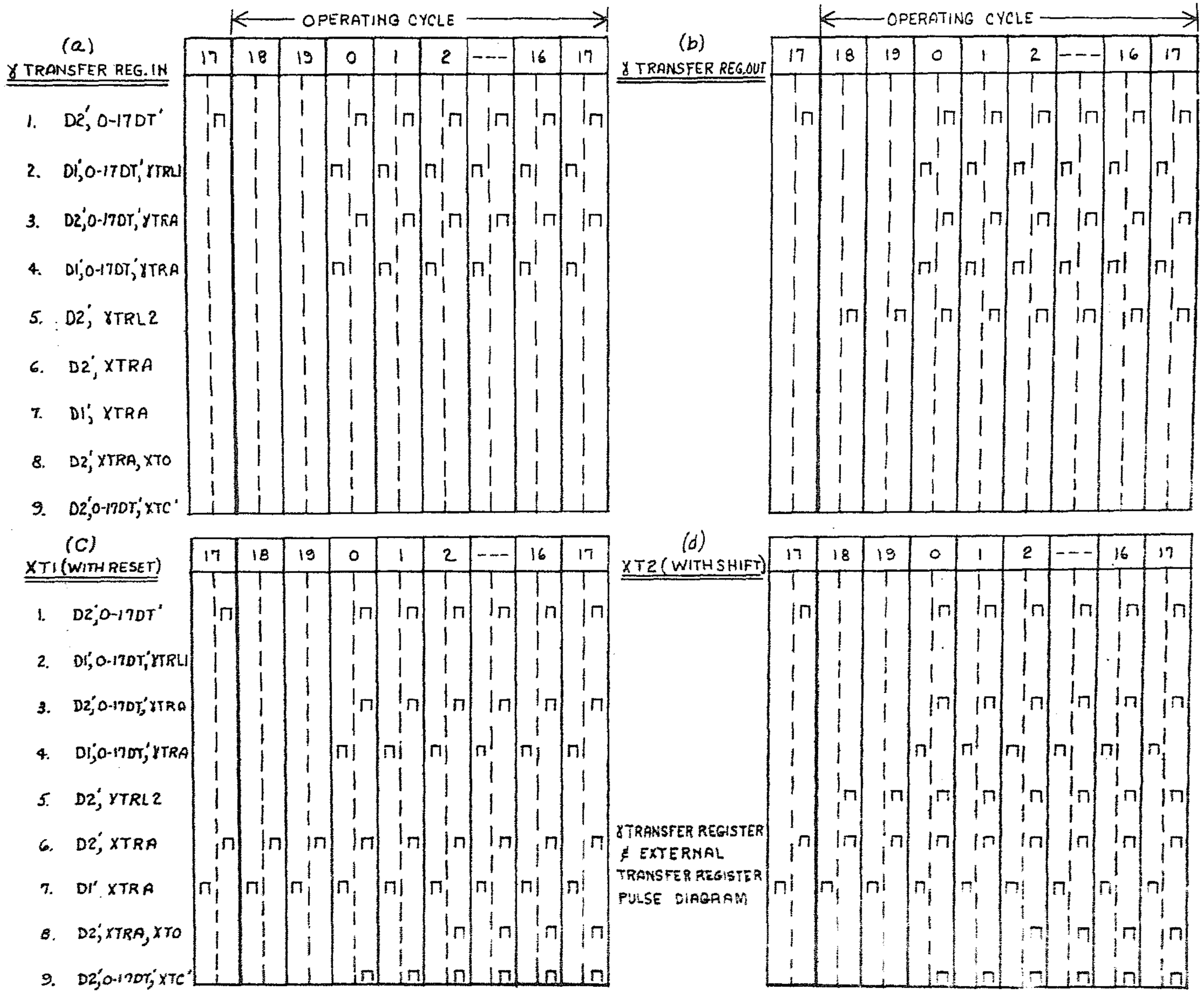


Fig. 4-55. Pulse Diagram for Y Transfer Register

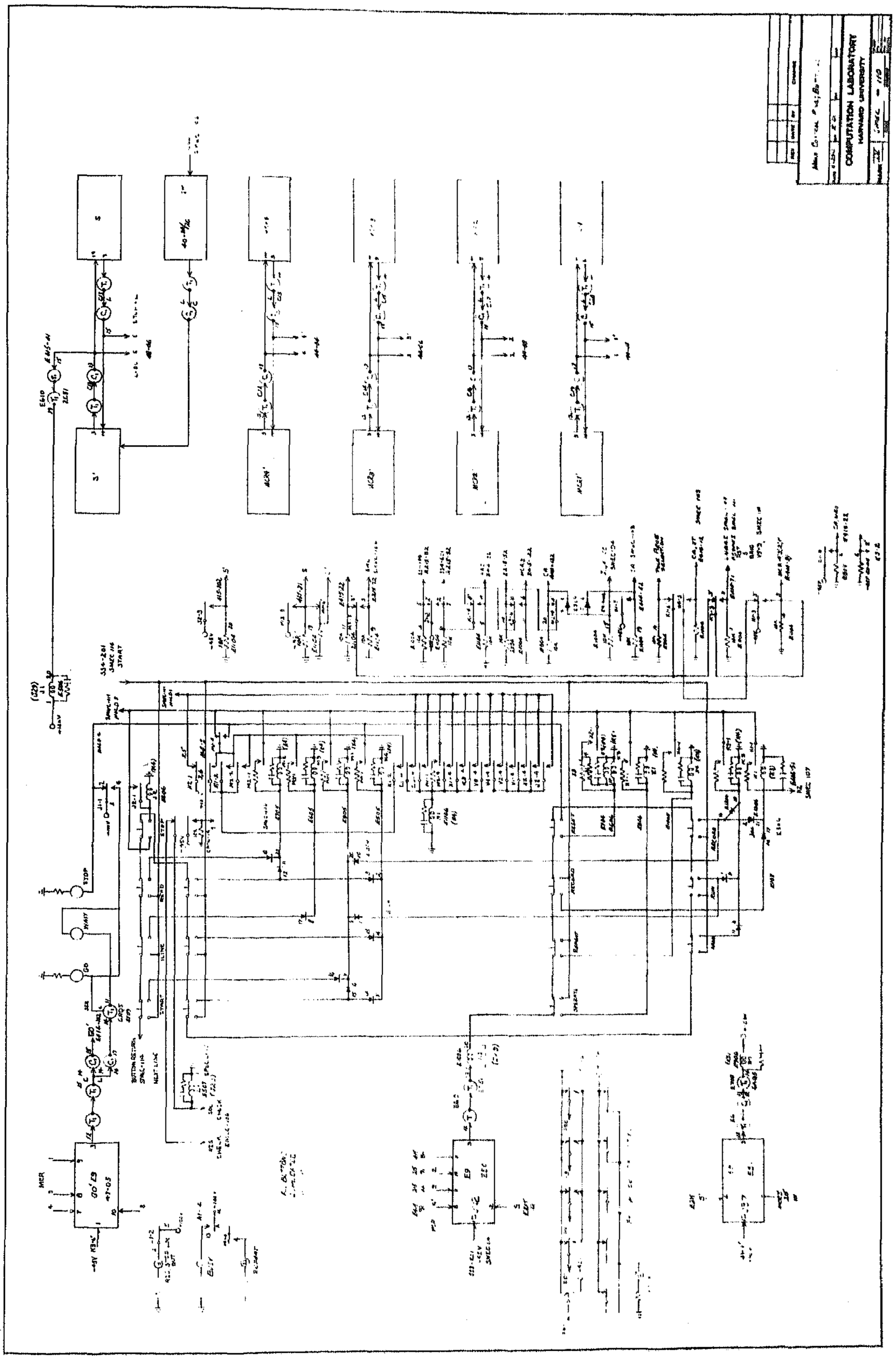


Fig. 4-56

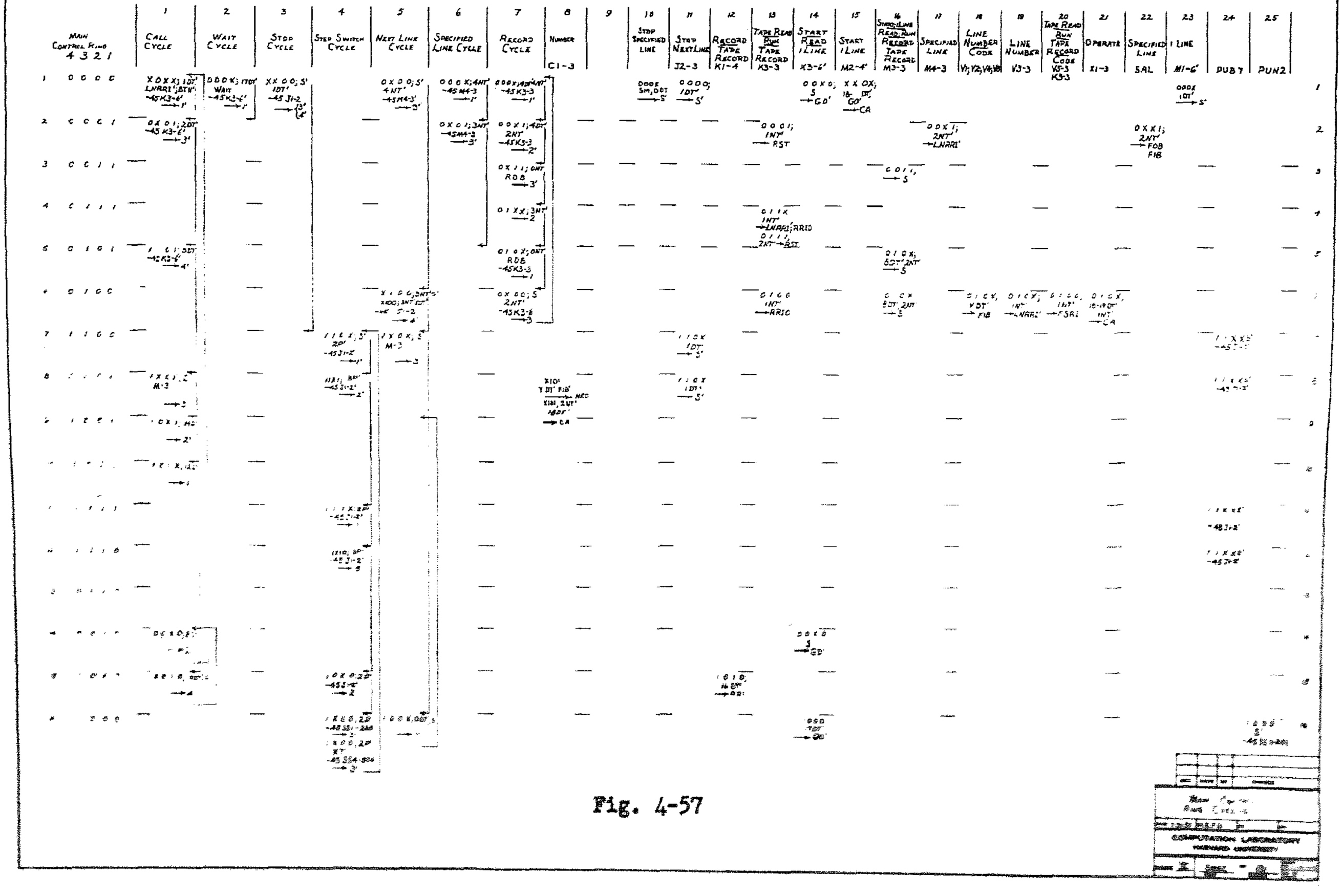

MAIN CONTROL FLAG 4321
1 CALL CYCLE
2 WAIT CYCLE
3 STOP CYCLE
4 STEP SWITCH CYCLE
5 NEXT LINE CYCLE
6 SPECIFIED LINE CYCLE
7 RECORD CYCLE
8 NUMBER C1-3
9
10 STOP SPECIFIED LINE
11 STOP NEXT LINE J2-3
12 RECORD TAPE RECORD K1-4
13 TAPE READ RUN TAPE RECORD K3-3
14 START READ 1 LINE X3-6'
15 START 1 LINE M2-4'
16 SPEC. LINE READ, RUN RECORD TAPE RECORD M3-3
17 SPECIFIED LINE M4-3
18 LINE NUMBER CODE V1 V2 V4 V8
19 LINE NUMBER V3-3
20 TAPE READ RUN TAPE RECORD CODE V5-3 K3-3
21 OPERATE X1-3
22 SPECIFIED LINE SAL
23 1 LINE M1-6'
24 DUB 7
25 PUN 2
COMPUTATION LABORATORY HARVARD UNIVERSITY

Fig. 4-57

MCR4 Type E9 SMEC-110

1.	Hold	MCR4 14					
2.	Call	MCR3; 11	MCR2'; 12	MCR1; 8	1ODT'; 10	S 9	

MCR4' Type E17 SMEC-110

1.	Hold	MCR4' 14					-45 V N1-3 1
2.	Next Line	MCR3'; 8	MCR2; 9	MCR1; 10	3NT'; 11	S' 12	-45 V (switch 4 6-7)
3.	Call	MCR3'; 15	MCR2; 16	MCR1'; 17	5DT' 18		-45 V K3-6' 5

MCR3',4' Type E9 SMEC-110

4.	Next Line	MCR3'; 8	MCR2; 9	MCR1; 10	3NT'; 11	5DT' 12	-45 V J1-2 1

MCR3',4'A Type E9 SMEC-110

5.	Stop	MCR2; 10	MCR1; 11	S'; 9	1DT' 12	-45 V J1-2 1

Connect MCR4' (6), MCR3'4'(3), MCR3'4'A(3).

Fig. 4-58

MCR3 Type E17 SMEC-110

1. Hold	MCR3 14					-45 V J1-2 (switch 8-9) 1
2. Call, Next Line	MCR4'; 8	MCR2; 9	M-3; 10	S 11		
3. Step Switch	MCR4; 15	MCR2'; 16	MCR1; 17	P3' 18		-45 V J1-2' 5

MCR2,3 Type E9

4. Read- Run-Rec	MCR4; 8	MCR2; 9	MCR1; 10	2NT'; 11	S 12	-45 V K3-6 run 1

Connect MCR3 (6), MCR2,3 (3).

Fig. 4-59 (cont. on next page)

MCR3'	Type E17						SMEC-110
1. Hold	MCR3' 14						-45 V N1-3 1
2. XT	MCR4'; 8	P2'; 9	MCR1; 10	MCR2; 11	XT 12		-45 V SS4-504 4
3. Step Switch	MCR4'; 15	MCR2; 16	MCR1; 17	P2' 18			-45 V SS1-220 5
MCR3'A	Type E9						
4. Call	MCR4; 8	MCR2; 9	MCR1'; 10	2DT' 11			-45 V K3-6' 1
MCR3'4'	Type E9						
5. Next Line	MCR4; 13	MCR2; 14	MCR1; 15	4NT'; 16	S' 17		-45 V M4-3' 20
MCR3'4'A	Type E9						
6. Stop	MCR2; 13	MCR1; 14	S'; 16	1DT' 15			-45 V J1-2 20
MCR1',3'	Type E9						
7. Spec. Line	MCR4; 8	MCR2; 9	MCR1'; 10	3NT' 11			-45 V M4-3 1 (switch 2-5)
MCR2',3'	Type E9						
8. Read-Run-Rec	MCR4; 8	MCR2'; 9	MCR1'; 10	RDB; 11	ONT' 12		

Connect MCR3'(6), MCR3'A(3), MCR3'4'(4), MCR3'4'A(4), MCR1'3'(3), MCR2'3'(3).

Fig. 4-59 (concluded)

MCR2	Type E17				SMEC-110
1. Hold	MCR2 14				
2. Step Switch	MCR4'; 8	MCR3; 9	MCR1; 10	P2' 11	-45 V J1-2' 4
3. Call	MCR4; 15	MCR3; 16	MCR1; 17	8DT' 18	

MCR2,3	Type E9			
4. Read-Run-Rec	MCR4; 13	MCR3'; 14	MCR1'; 15	3NT' 16

Connect MCR2(6), MCR2,3(4)

MCR2'	Type E17				SMEC-110
1. Hold	MCR2' 14				-45 V N1-3 1
2. Step Switch	MCR4'; 8	MCR3'; 9	MCR1'; 10	P3' 11	-45 V J1-2' 4
3. Call	MCR4'; 15	MCR3; 16	MCR1'; 17	14DT' 18	

MCR2'3'	Type E9					
4. Read-Run-Rec	MCR4; 13	MCR3; 14	MCR1'; 15	2NT'; 16	4DT' 17	-45 V K3-3 20

Connect MCR2'(6), MCR2'3'(4)

Fig. 4-60

MCR1	Type E17						SMEC-110
1. Hold	MCR1 14						
2. Step Switch	MCR4'; 8	MCR3'; 9	MCR2'; 10	P2' 11			-45 V J1-2' 4
3. Call	MCR4'; 15	MCR3; 16	MCR2'; 17	12DT' 18			
MCR1A	Type E9						SMEC-110
4. Read-Run-Rec	MCR4; 8	MCR3'; 9	MCR2; 10	ONT'; 11	RDB 12		-45 V K3-3 1
	Connect MCR1(6), MCR1A(3).						
MCR1'	Type E17						SMEC-110
1. Hold	MCR1' 14						-45 V N1-3 1
2. Step Switch	MCR4'; 8	MCR3'; 9	MCR2; 10	P2'; 11	S' 12		-45 V J1-2' 4
3. Call	MCR3; 15	LNRRI'; 16	βT11'; 18	1DT' 19			-45 V K3-6' 5
MCR1'A	Type E9						
4. Read-Run-Rec	MCR4; 8	MCR3; 9	MCR2; 10	4NT' 11			-45 V K3-3 1
5. Wait	MCR4; 13	MCR3; 14	MCR2; 15	Wait; 16	17DT' 17		-45 V K3-6' 20

Fig. 4-61 (cont. on next page)

MCR1'3' Type E9 SMEC-110

6.	Spec. Line	MCR4; 13	MCR3; 14	MCR2; 15	4NT'; 16	S' 17	-45 V M4-3 20

MCR1A Type E9 SMEC-110

7.	Next Line	MCR4'; 13	MCR3; 14	MCR2; 15	ODT'; 16	S 17

Connect MCR1'(3), MCR1'A(3), MCR1'A(4), MCR1'3'(4), MCR1A(4).

Fig. 4-61 (concluded)

S Type E17 SMEC-110

1.	Hold	S 14					-45 V N1-3 1
2.	One Line	MCR4; 8	MCR3; 9	MCR2'; 10	MCR1' 11		-45 V M3-3 4
3.	One Line	MCR4; 15	MCR3'; 16	MCR2; 17	2NT'; 18	8DT' 19	-45 V M3-3 5

Fig. 4-62 (cont. on next page)

S'	Type E17						
1. Hold	S' 14						
2. Rec. Check LN	LNRRI'; 8	FIB4; 9	D_1'; 10	IDT' 11			-45 V K3-3 4
3. Rec. Check Code	FSRI'; 15	FIB4'; 16	IDT' 17				-45 V K3-3 5
S'A	Type E9						
4. 1 Line	MCR4; 8	MCR3; 9	MCR2; 10	IDT' 11			-45 V M1-6' 1
5. Stop Spec. Line	MCR4; 17	MCR3; 16	MCR2; 15	SM; 14	ODT' 13		-45 V Stop Switch 20
S'B	Type E17						
6. Code Stop	FIB8'; 8	IDT'; 9	βH3'; 10	βT1'; 11	βU12' 12		GND 1
7. Check Stop	FIB8'; 15	IDT'; 16	βH3'; 17	βT1'; 18	βU13' 19		
S'C	Type E9						
8. Button Stop	MCR:4'; 8	3'; 9	2; 10	IDT' 11			-45 V J2-3 1
9. Button Stop	MCR:4; 13	3; 14	2; 15	1; 16	IDT' 17		-45 V J2-3 20
S'D	Type E21						
10. Read Check	IDT'; 11	GO'; 12	RCD; 10	MCR2 9			
11. Read mech.	IDT'; 20	GO'; 4	RDMC; 5	MCR2 6			
12. Record mech.	IDT'; 16	GO'; 14	RCMC; 15	MCR2 13			

Connect S'A(3), S'B(6), S'D(3). Connect S'(6), S'B(3), S'C(3), S'C(4).

Fig. 4-62 (concluded)

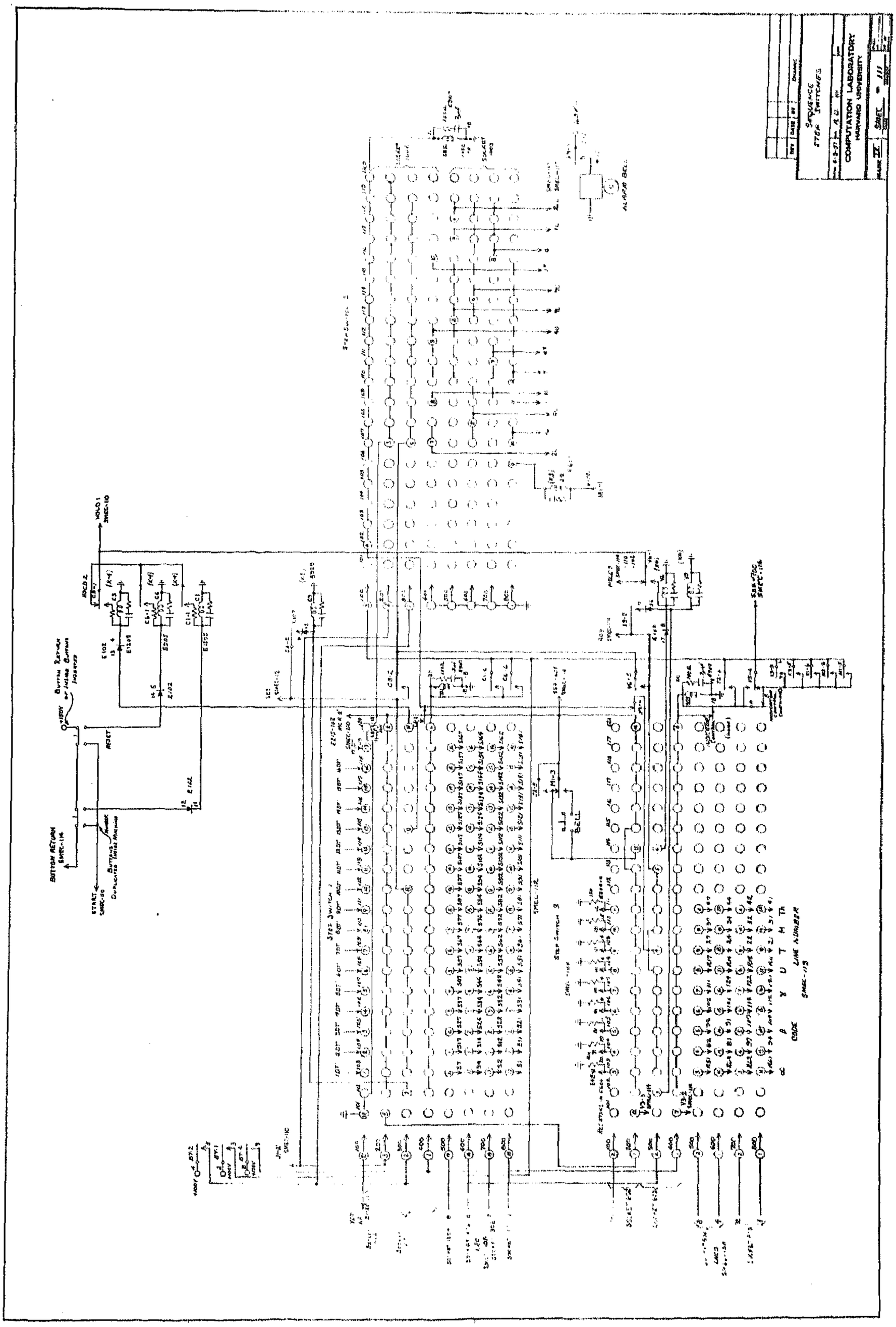

SEQUENCE
FIVE SWITCHES
COMPUTATION LABORATORY
HARVARD UNIVERSITY
BUTTON RETURN
START
BELL
CODE
LINE NUMBER

Fig. 4-63

GO'	Type E9					SMEC-110
1.	MCR4; 11	MCR3; 8	MCR1; 9	S 10		-45 V K3-6' 1
2.	MCR4'; 13	MCR3; 14	MCR2; 15	MCR1; 10	17DT' 17	-45 V K3-6' 20

Fig. 4-64

PUN2	Type E9					SMEC-110
1. SS	MCR4'; 8	3; 9	2; 10	1; 11	S' 12	SMEC-114 -45 V SS3-201 1

PUB7	Type S9					SMEC-110
1. Step Switch	MCR4'; 10	MCR3'; 11	S' 12			-45 V J1-2' 1

RR1	Type E9					SMEC-107
1. Read-Run-Rec	MCR:4'; 8	3; 9	2'; 10	1; 11	16DT'; 12	-45 V K1-4 1

Fig. 4-65

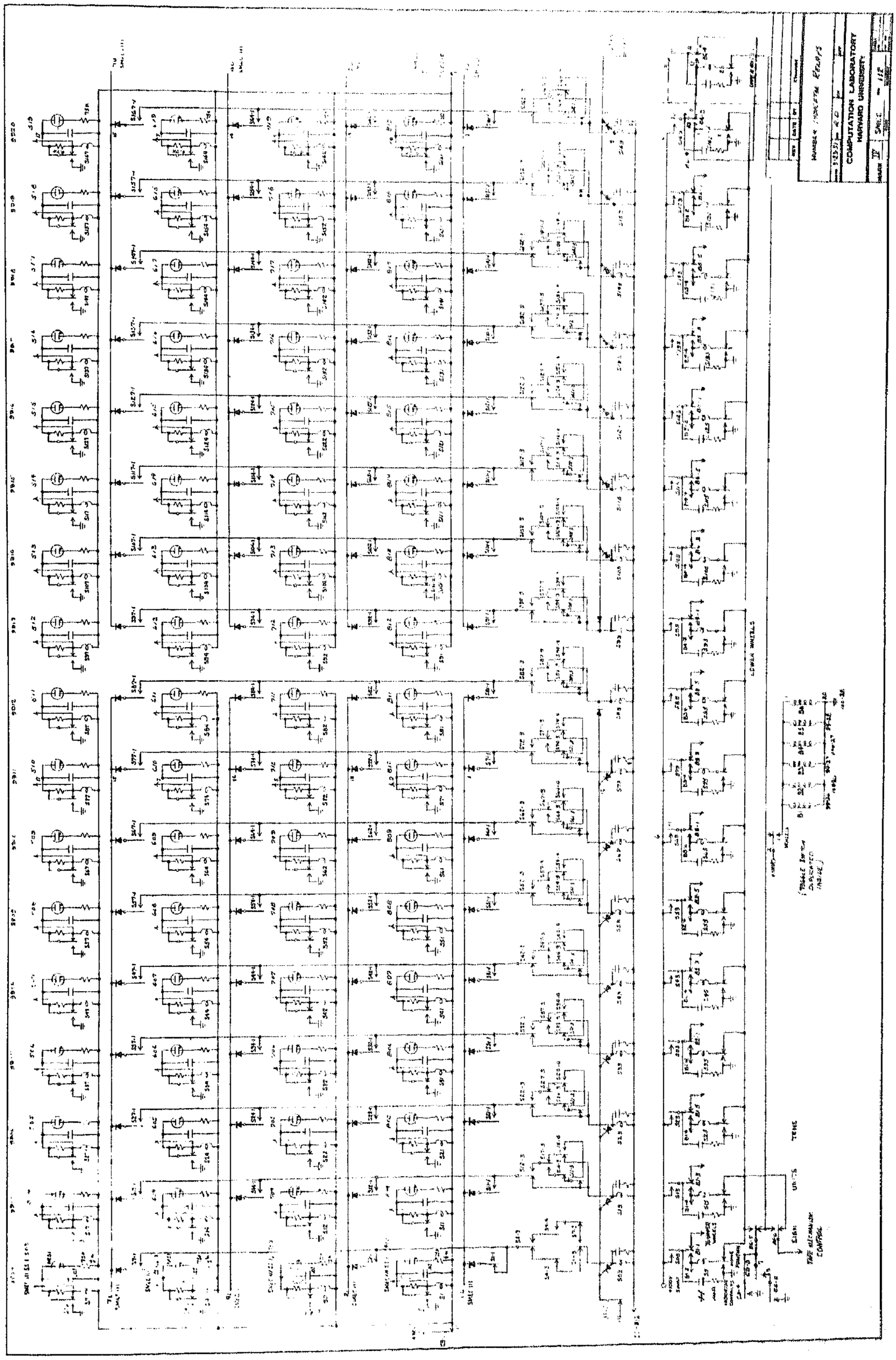


Fig. 4-66

NRO4	Type E20					SMEC-108
1. Hold	NRO-4'; 14	MCR3' 13				-45 V C1-3' 1
2. Bus	FIB4'; 8	MCR3'; 9	MCR2; 10	MCR1'; 11	YDT' 12	

Fig. 4-67

LNCO-8	Type E14	SMEC-108
1. FSTP 1' A1		-45 V SS3-103 B3
2. FSTP 5' A5		-45 V SS3-104 B4
3. FSTP 9' A9		-45 V SS3-105 B5
4. FSTP 13' A13		-45 V SS3-106 B6
5. FSTP 17' A17		-45 V SS3-107 B7
6. LNRU8' B15		-45 V SS3-108 B8
7. LNRT8' B19		-45 V SS3-109 B9
8. LNRHO3'; C13	LNRHE4'; C14	-45 V SS3-110 B10
9. LNRHE8' C8		-45 V SS3-110 B10
10. LNRHO-9' C19		-45 V SS3-110 B10
11. LNRTHO-8' C1		-45 V SS3-111 B11

Fig. 4-68

Decimal Digit	Binary Notation	Number of Pulses to Indicator
0	0 1 0 1	5
1	0 0 0 1	1
2	0 0 1 0	2
3	1 0 0 1	8
4	0 1 0 0	4
5	0 1 1 0	6
6	0 0 1 1	3
7	1 0 1 0	9
8	1 0 0 0	7
9	1 1 0 0	10
+	0 0 0 0	1
-	1 0 0 0	7
S	0 1 1 1	2

Position	Order on Indicators	
	Digits	Sign
Home	Blank	Blank
1	1	+
2	2	S
3	6	Blank
4	4	↓
5	0	
6	5	
7	8	-
8	3	Blank
9	7	↓
10	9	

Fig. 4-69

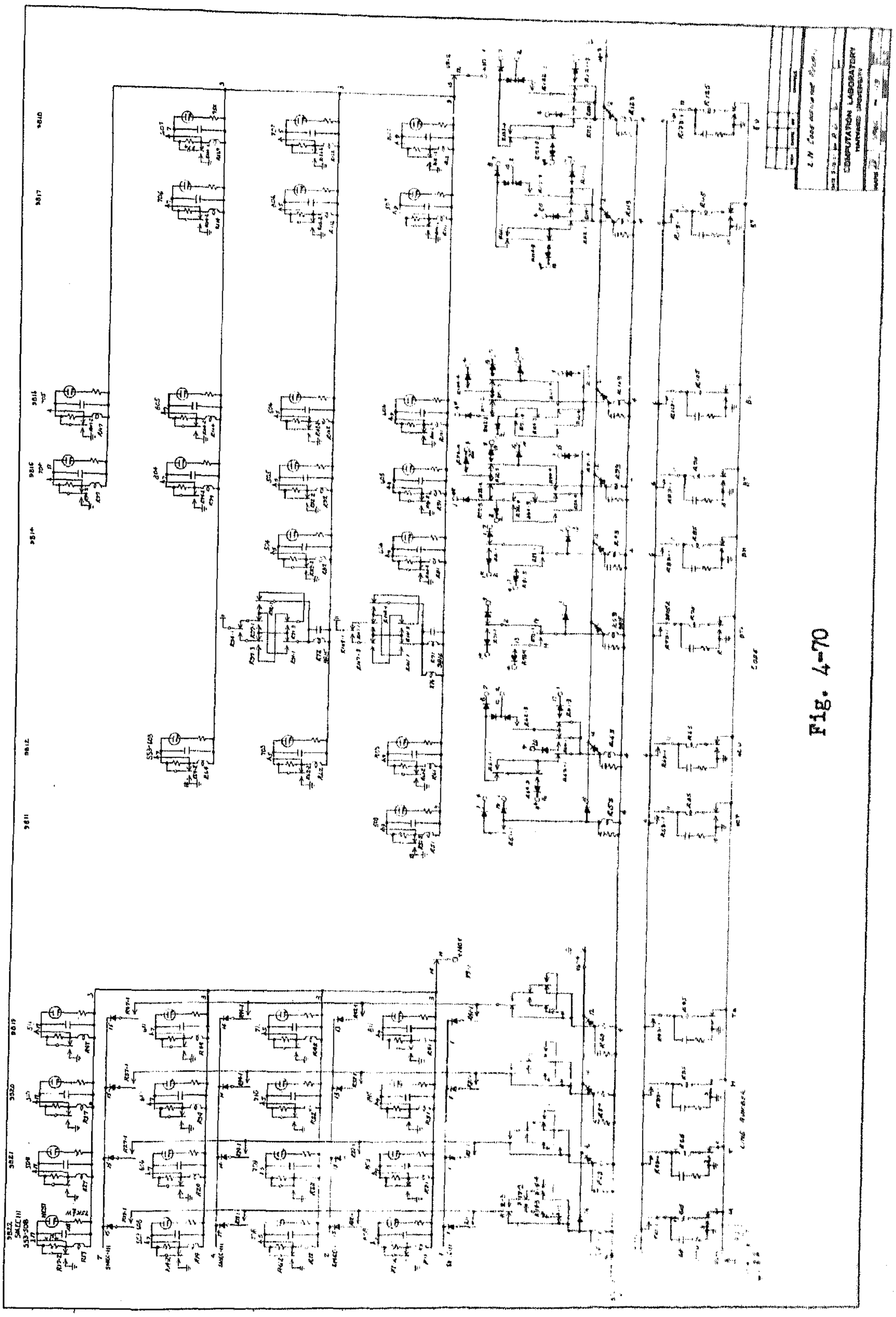


Fig. 4-70

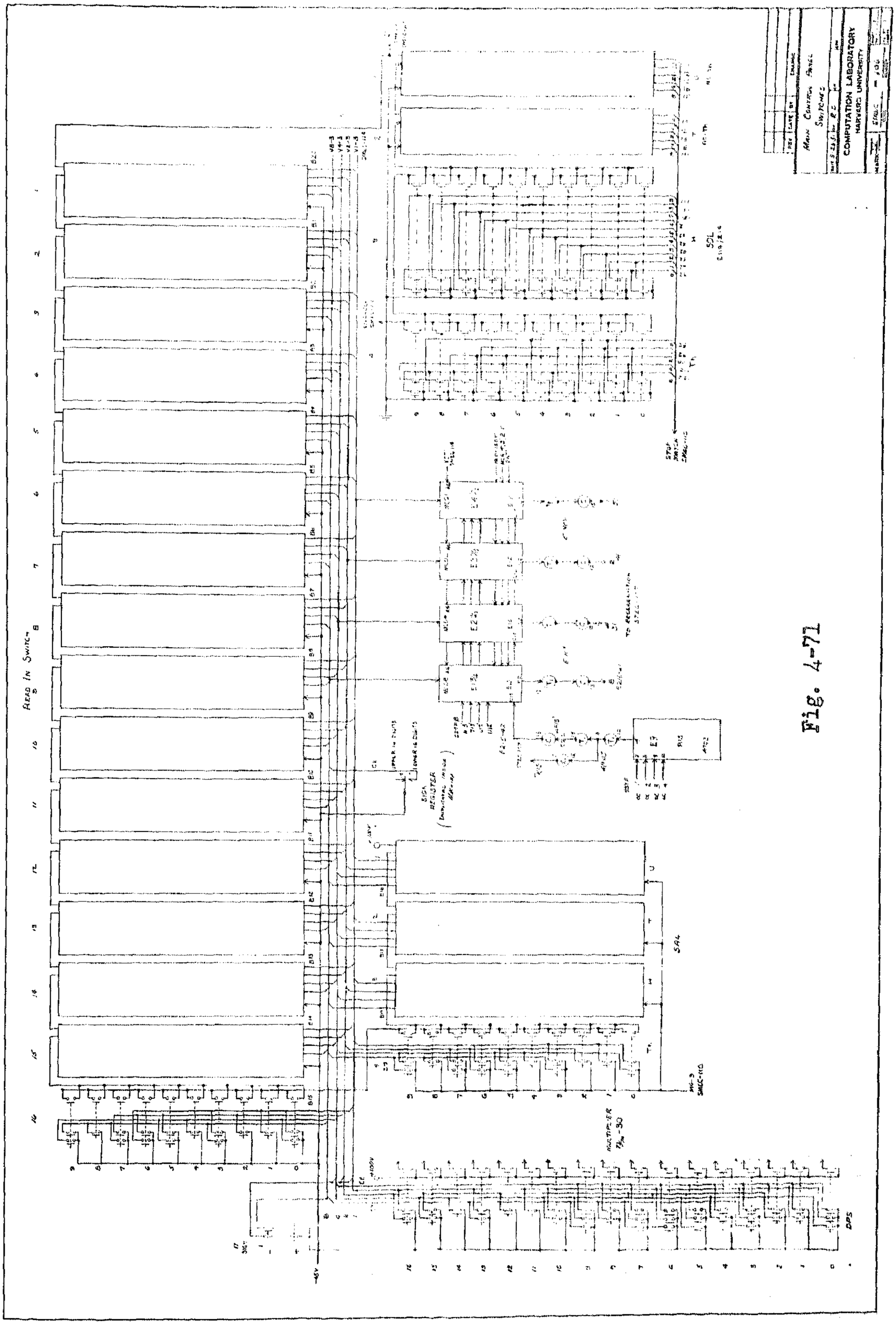

COMPUTATION LABORATORY
HARVARD UNIVERSITY
MAIN CONTROL PANEL
SWITCHES
READ IN SWITCH
SAL
SAA
DPS
MULTIPLIER
TYPE - 30

Fig. 4-71

MCO-8 Type E12 SMEC-106

1.	RIS	RIS' C13	ODT' A20	-45 V	RIS 8,1 B20
2.	"		1DT' A1	-45 V	RIS 8,2 B1
3.	"		2DT' A2	-45 V	RIS 8,3 B2
4.	"		3DT' A3	-45 V	RIS 8,4 B3
5.	"		4DT' A4	-45 V	RIS 8,5 B4
6.	"		5DT' A5	-45 V	RIS 8,6 B5
7.	"		6DT' A6	-45 V	RIS 8,7 B6
8.	"		7DT' A7	-45 V	RIS 8,8 B7
9.	"		8DT' A8	-45 V	RIS 8,9 B8
10.	"		9DT' A9	-45 V	RIS 8,10 B9
11.	"		10DT' A10	-45 V	RIS 8,11 B10
12.	"		11DT' A11	-45 V	RIS 8,12 B11
13.	"		12DT' A12	-45 V	RIS 8,13 B12
14.	"		13DT' A13	-45 V	RIS 8,14 B13
15.	"		14DT' A14	-45 V	RIS 8,15 B14
16.	"		15DT' A15	-45 V	RIS 8,16 B15

Fig. 4-72 (cont. on next page)

MCO-8 (continued)

17.	SAL	MCR4;1'; C8 C9	ODT'; A20	2NT'; C10		-45 V	SAL 8,1 B16
18.	"	"	1DT'; A1	"		-45 V	SAL 8,2 B17
19.	"	"	2DT'; A2	"		-45 V	SAL 8,3 B18
20.	"	"	3DT'; A3	"		-45 V	SAL 8,4 B19
21.	SS4	MCR4;3'; C8 C12	2; C11	XDT'V3-5; A16		-45 V	V8-3 C4
22.	DPS	βH3'; C15	βT13'; C16	βU13'; C17	ODT'; A20	-45 V	DPS 8 C7
23.	SIGN	βH3'; C15	βT13'; C16	βU12' C19	19DT'; A17	-45 V	SIGN C6
24.	RIS	RIS'; C13	19DT'; A19			-45 V	RIS 8,0 C5

Fig. 4-72 (concluded)

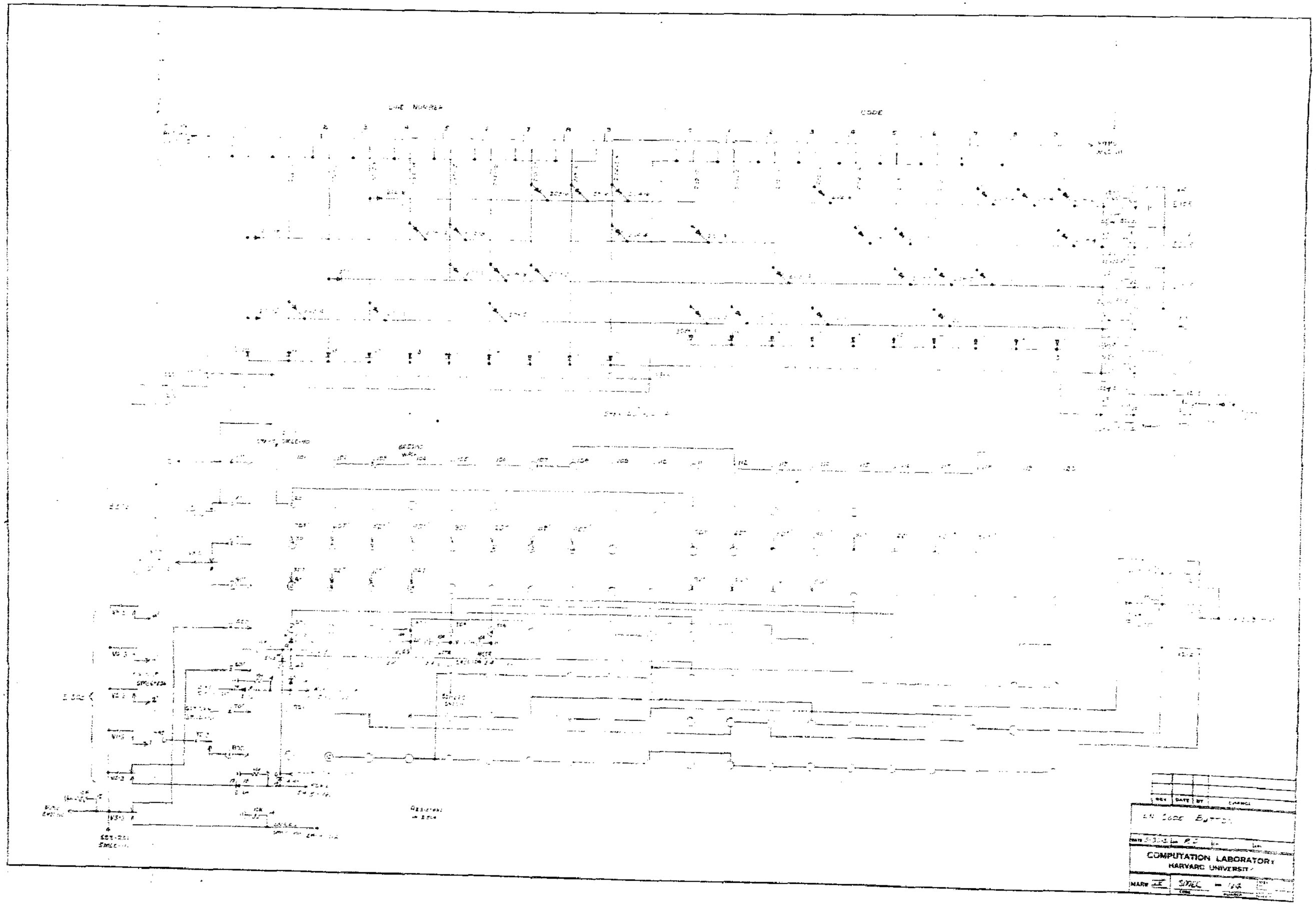

LINE NUMBER
CODE
COMPUTATION LABORATORY
HARVARD UNIVERSITY

Fig. 4-73

RIS' Type E9 SMEC-106

1. SSTP:a1'; a2; a3; a4
13 14 15 16

Fig. 4-74

SM Type E11 SMEC-110

LNRTHO-8' or C11	SOL4-8; C12	LNRTHO-4' or C13	SOL4-4; C14	LNRTHO-2' or C15	SOL4-2; C16
LNRTHO-1' or C17	SOL4-1; C18	LNRTHO-0' or C19	SOL4-0; C20	LNRHO-9' or B11	SOL3-9; B12
LNRHO-7' or B13	SOL3-7; B14	LNRHO-5' or B15	SOL3-5; B16	LNRHO-3' or B17	SOL3-3; B18
LNRHO-1' or B19	SOL3-1; B20	LNRHE-8' or C8	SOL3-8; C9	LNRHE-6' or B3	SOL3-6; B4
LNRHE-4' or B5	SOL3-4; B6	LNRHE-2' or B7	SOL3-2; B8	LNRHE-0' or B9	SOL3-0; B10
LNRT-8' or A11	SOL2-8; A12	LNRT-4' or A13	SOL2-4; A14	LNRT-2' or A15	SOL2-2; A16
LNRT-1' or A17	SOL2-1; A18	LNRT-0' or A19	SOL2-0; A20	LNRU-8' or C6	SOL1-8; C7
LNRU-4' or A3	SOL1-4; A4	LNRU-2' or A5	SOL1-2; A6	LNRU-1' or A7	SOL1-1; A8
LNRU-0' or A9	SOL1-0. A10				

Fig. 4-75

MCTR Type E10 SMEC-104

1.	Hold	MCTR 14			
2.	Reset (drum)	17DT'; 11	GO' 12		
3.	Reset	5DT'; 8	GO' 9		

MA Type S9 SMEC-104

4.	Reset (read-in)	(17-1)DT'; 11	FSRI' 12		-45 V SS4-501 1
5.	Reset	12DT'; 14	FSRI' 13		-45 V SS4-506 20

Connect MCTR(3), MA(3), MA(4)

MCTR' Type E10 SMEC-104

1.	Hold	MCTR' 14			
2.	Drum	Drum'; 10	2DT' 11		
3.	Bus	FIB4; 6	1'; 7	7DT'; 8	FSRI' 9

Fig. 4-76

Button	Hold 1 N2-2'	Hold 2 N2-2',C3-1'	Hold 3 N2-2',V6-1'	Hold 4 J1-1'	
Number	N1;C3	C1			SS1,SS2;
Reset	N1;C3	C6			C9
Next Line:					
Start	N1;V6		M1	M3	
One Line	N1;V6		M3		
Read	N1;V6		M2;M3		
Stop	N1;V6		J2		
Spec. Line:					
Start	N1;V6		M1	M3;M4	
One Line	N1;V6		M3	M4	
Read	N1;V6		M2;M3	M4	
Line Number	N1;V6		V8;V4;V2;V1;V3		SS2;SS3;
Code	N1;V6		V8;V4;V2;V1;V5	SS4	V9
Operate	N1;V6		X1		
Repeat			X4		
Record	N1;V6		K1;M3		
Reset	N1;V6		X2;X3	SS4	
Read Seq.Tape	N1;V6		K3		
Run Seq. Tape	N1;V6		K3;M1	M3	
Rec. Seq.Tape	N1;V6		K1;K3;M1	M3	

Fig. 4-77

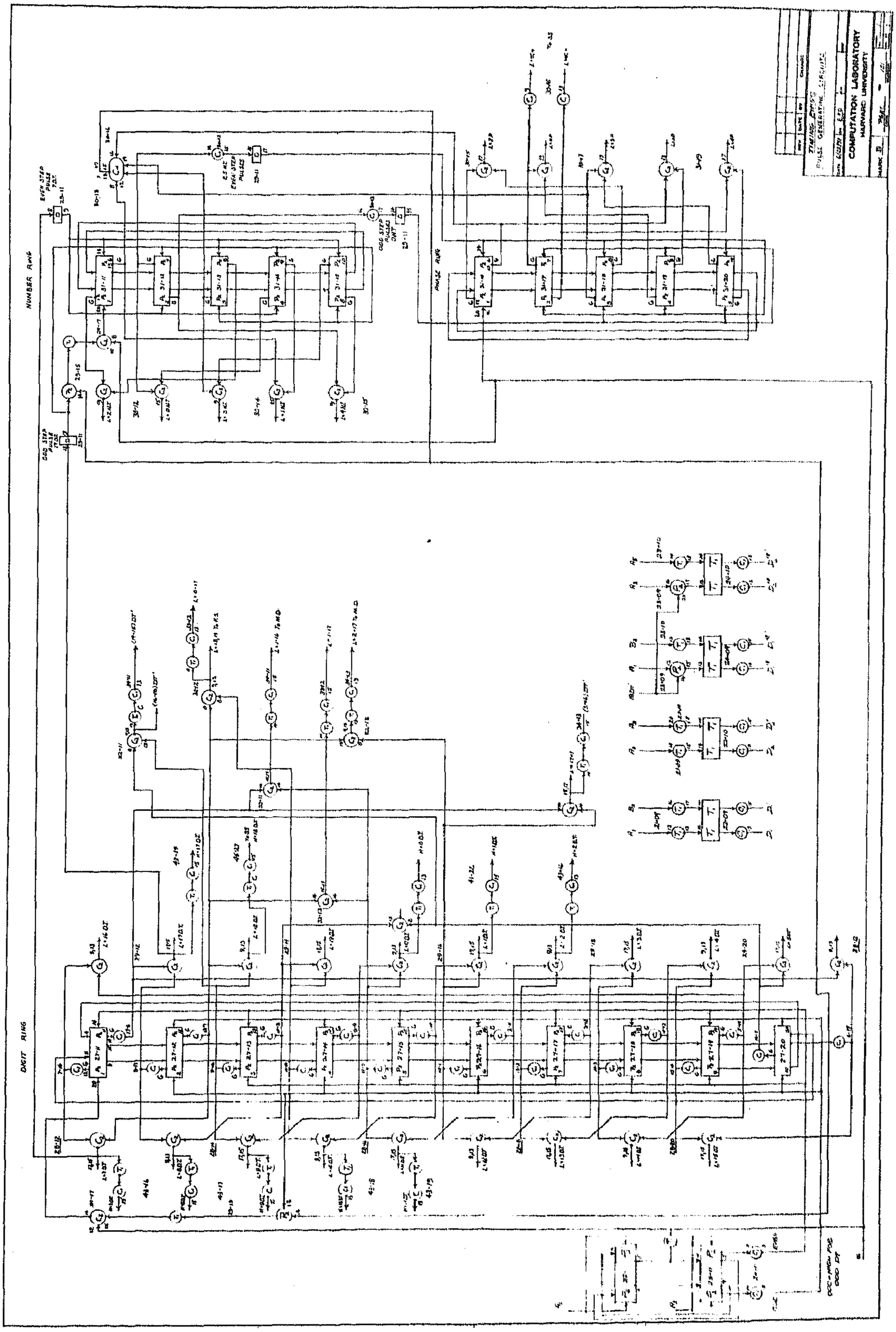
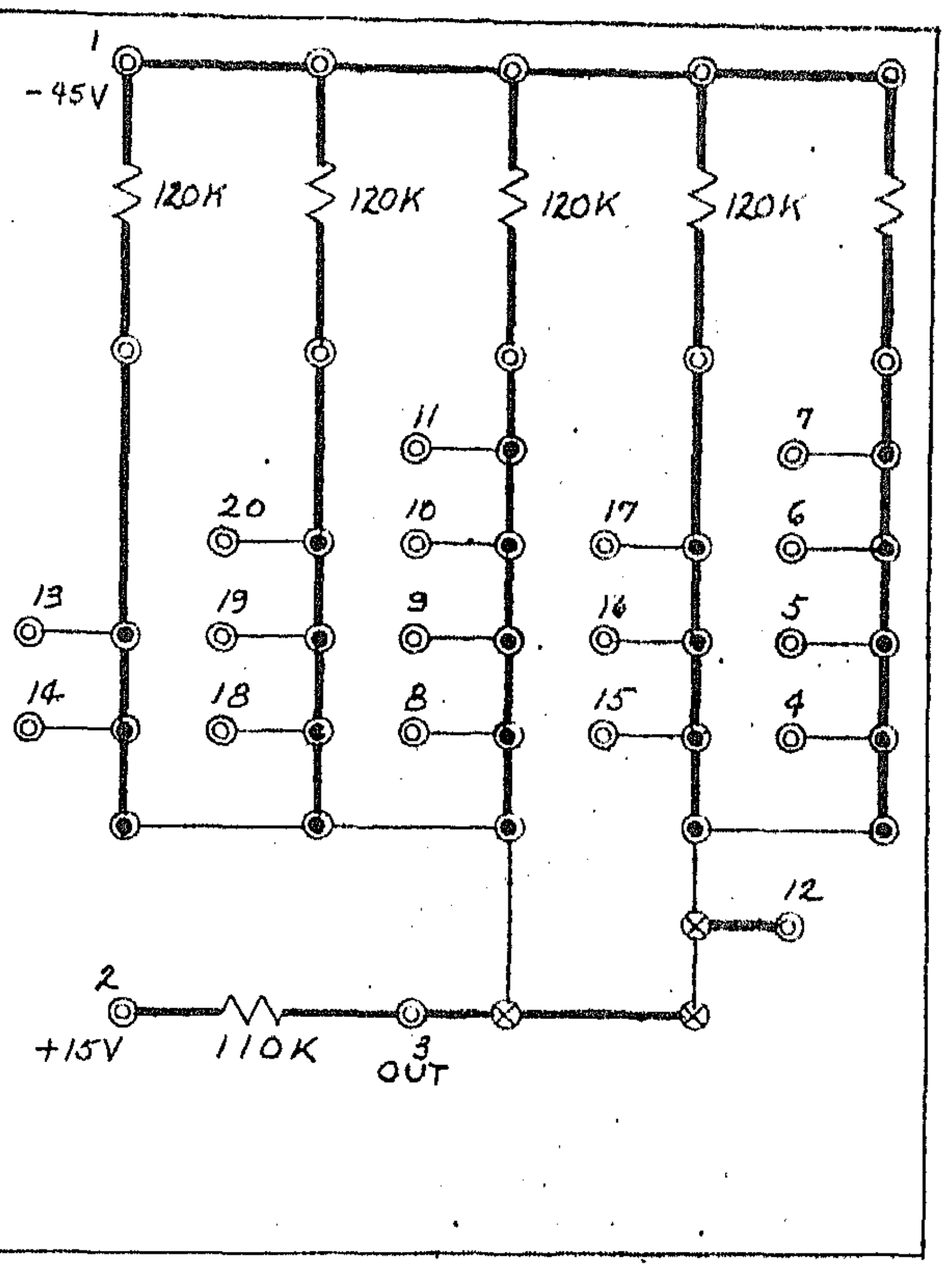

COMPUTATION LABORATORY
HARVARD UNIVERSITY
NUMBER RING
ANGLE RING
DIGIT RING

Fig. 4-78



LEGEND.

- ● BRIGHT SIDE OF RECTIFIER
- ⊗ DULL SIDE OF RECTIFIER
- ◎ TERMINAL EYELET
- —— BACK CONNECTION
- ▬▬ FRONT CONNECTION

NOTE.

USE 0.4 TO 0.6 ma.
FORWARD CURRENT RECTIFIERS

[2, 3, 9, 1 X (3, 9)]

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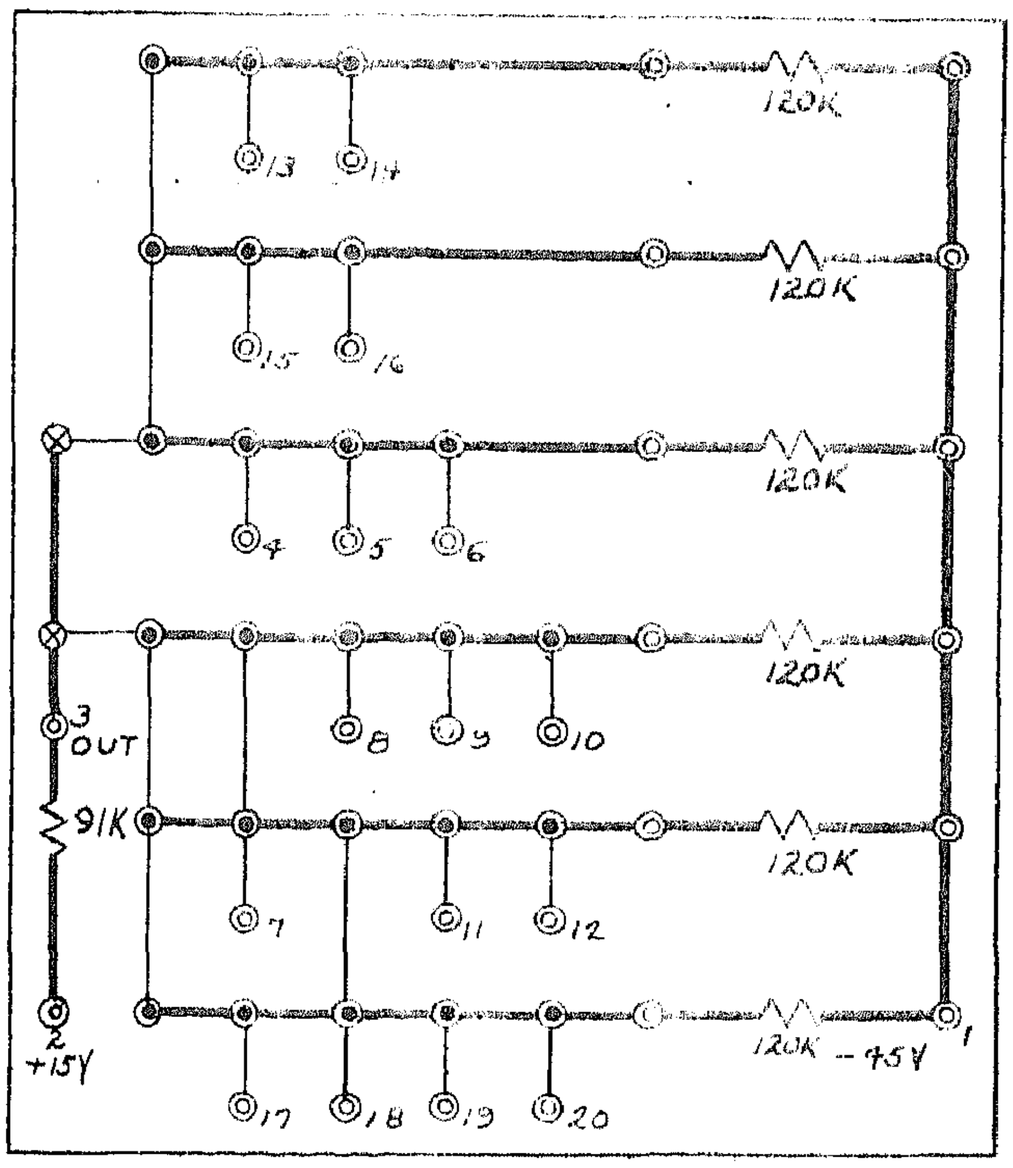
MARK IV	CC (CODE) — E-3 (NUMBER)	SHEET NO.	NO. OF SHEETS

Fig. 4-79



LEGEND.

- ◉ BRIGHT SIDE OF RECTIFIER
- ⊗ DULL SIDE " "
- ◎ TERMINAL EYELET
- —— BACK CONNECTION
- ▬▬ FRONT "

NOTE.

USE 0.9 TO 0.6 ma. FORWARD CURRENT RECTIFIERS

(2,2,3,4,4,4)

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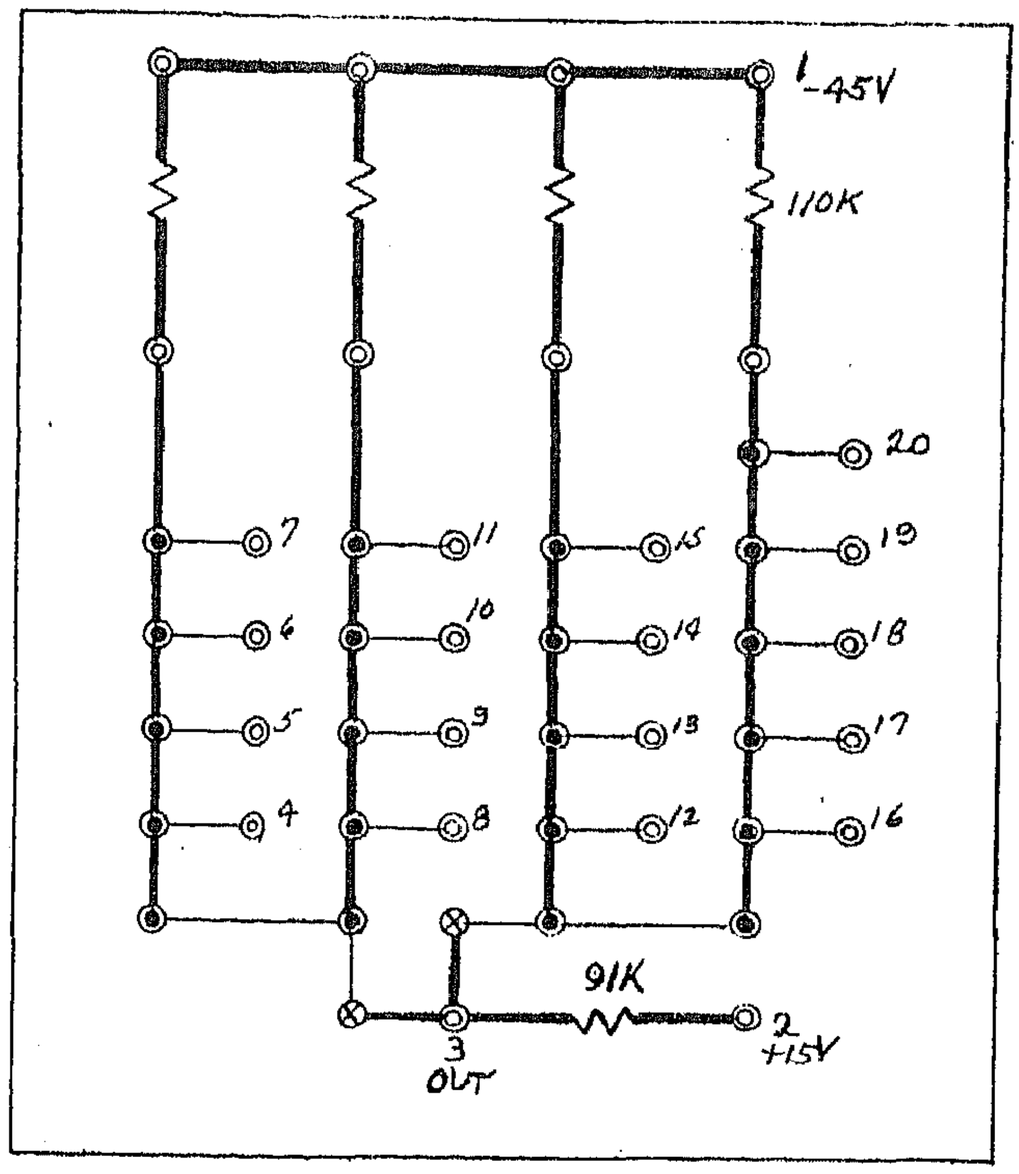
MARK IV	CC — E-5	SHEET NO.
	CODE NUMBER	NO. OF SHEETS

Fig. 4-80



(8885)

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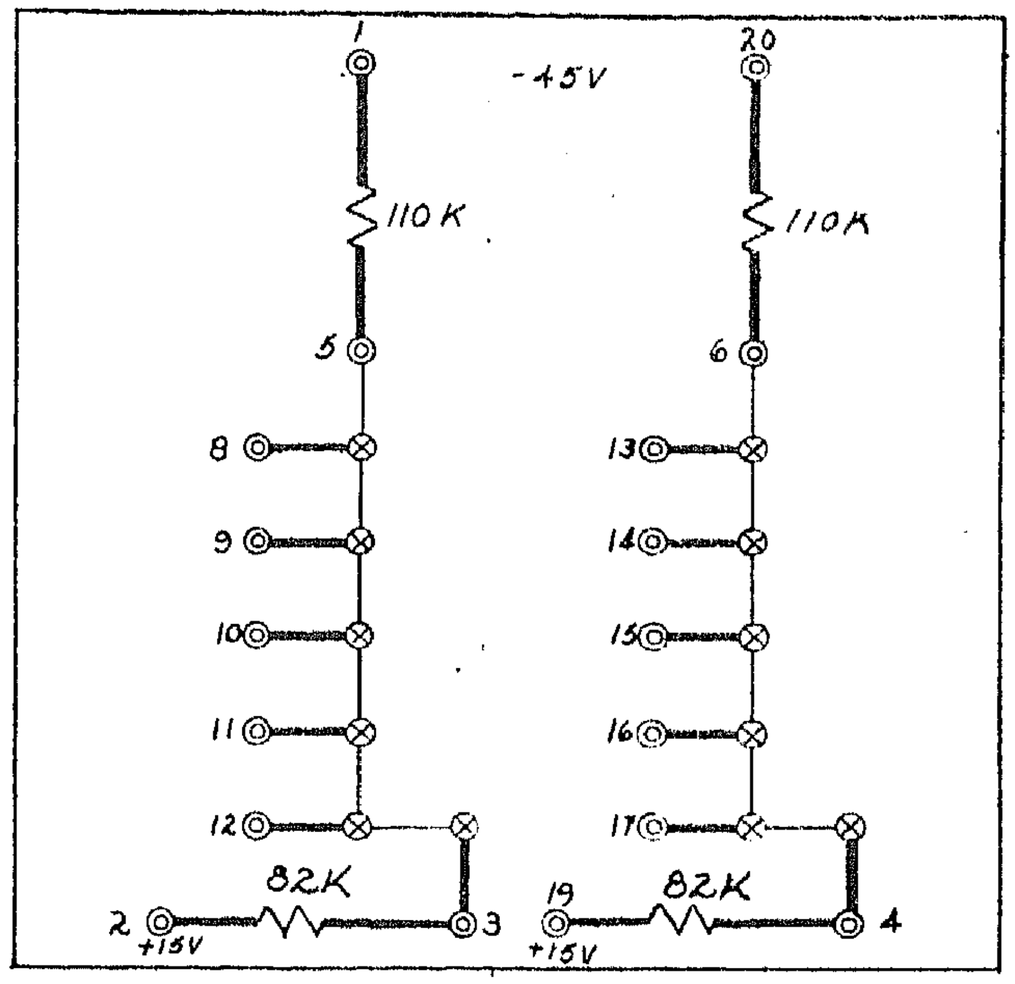
MARK IV	CC CODE	E-7 NUMBER	SHEET NO. / NO. OF SHEETS

Fig. 4-81



LEGEND:

- ◉ BRIGHT SIDE OF RECTIFIER
- ⊗ DULL SIDE OF RECTIFIER
- —— BACK CONNECTION
- ▬▬ FRONT CONNECTION

NOTE:

USE 0.4 TO 0.6 MA
FORWARD CURRENT
RECTIFIERS

(5) (5)

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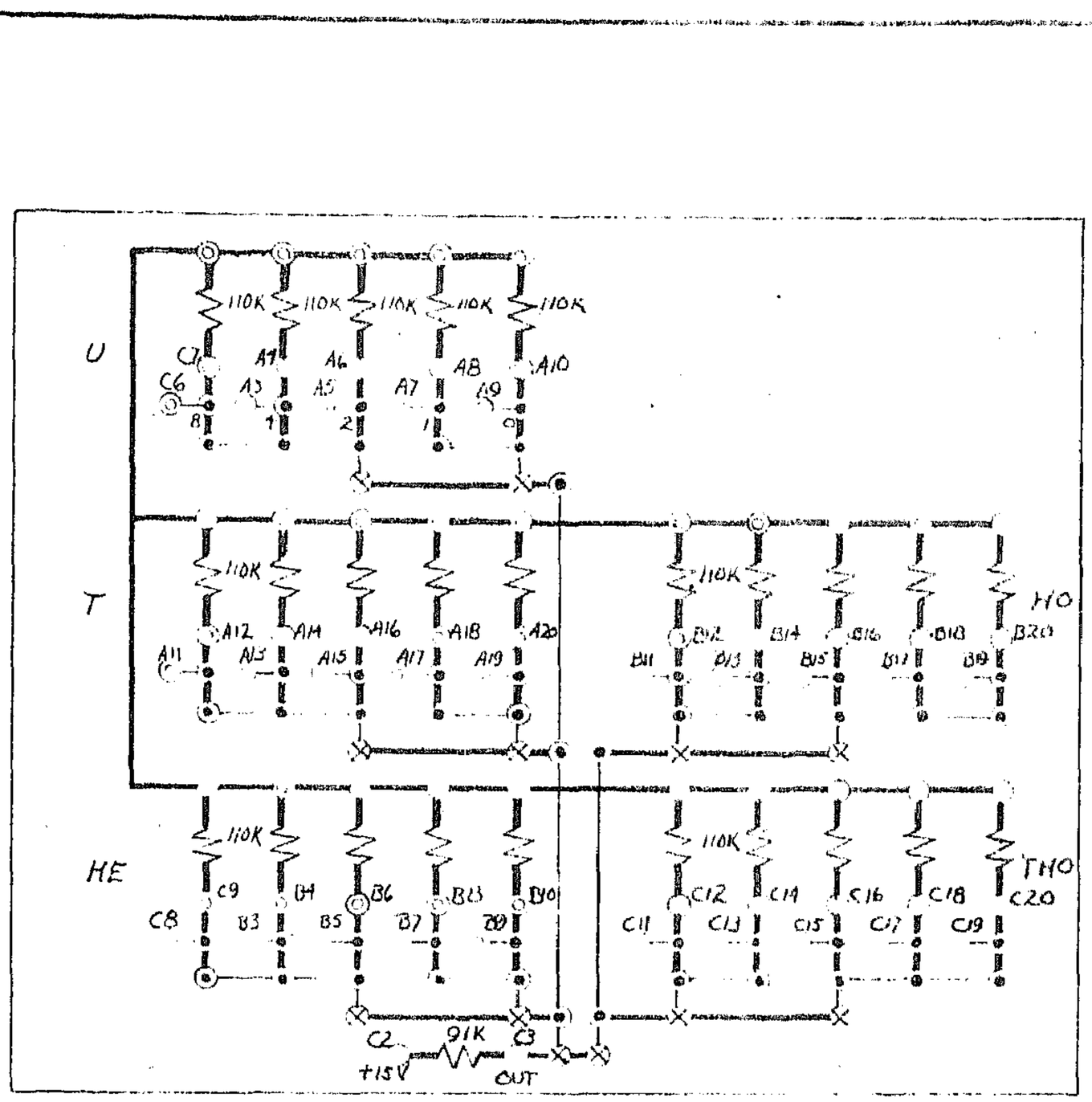
MARK IV	CC — E-9a (CODE — NUMBER)	SHEET NO. 1
		NO. OF SHEETS 1

Fig. 4-82



LEGEND:

——— FRONT CONNECTION

——— BACK CONNECTION

◉ BRIGHT SIDE OF RECTIFIER

⊗ DULL SIDE OF RECTIFIER

◎ TERMINAL EYELET

(SM)

DATE 7-27-51	DR. E.F.D	CH.	APP.

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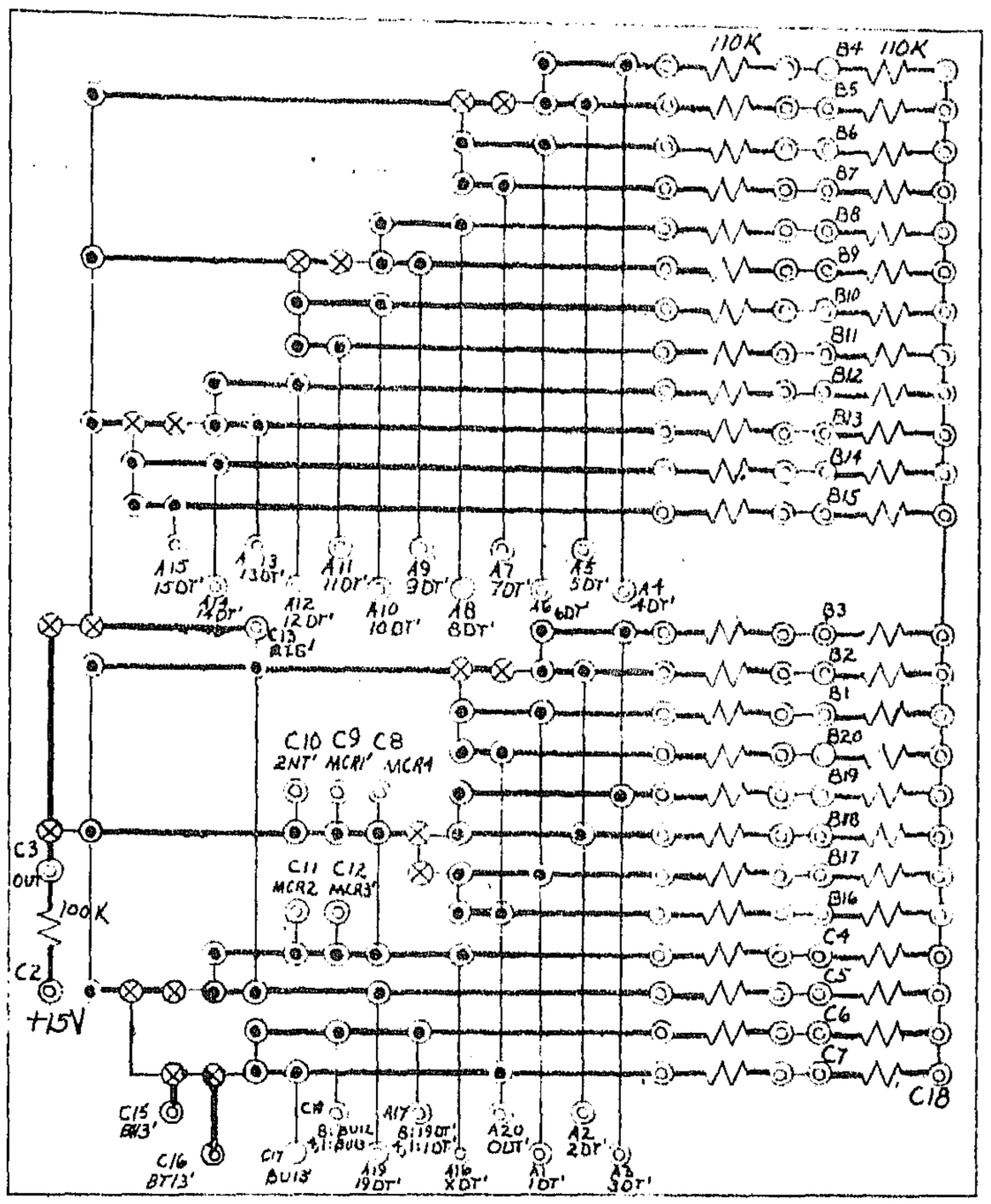
MARK IV	CC — E11 (CODE — NUMBER)	SHEET NO / NO. OF SHEETS

Fig. 4-83



LEGEND:

——— BACK CONNECTION

▬▬ FRONT CONNECTION

◉ BRIGHT SIDE OF RECTIFIER

⊗ DULL SIDE OF RECTIFIER

◎ TERMINAL EYELET

MCO

NOTE: USE 0.4 TO 0.6 ma FORWARD CURRENT RECTIFIERS

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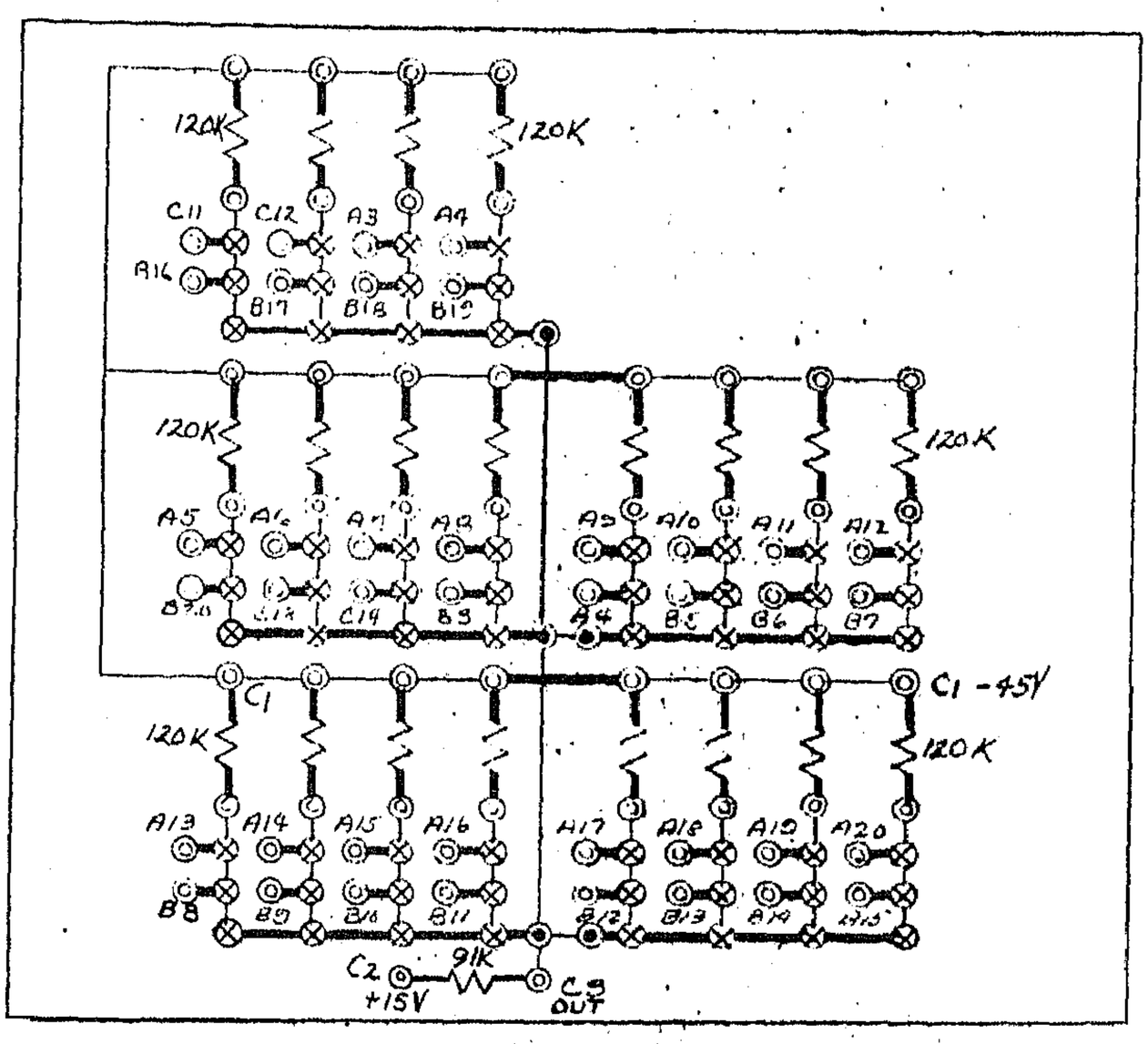
MARK IV	CC (CODE)	E12 (NUMBER)	SHEET NO. 1 / NO. OF SHEETS 1

Fig. 4-84



REC.
A = FSTP'
B = DT'

DATE: 5-18-51	DR. R.D.	CH.	APP.

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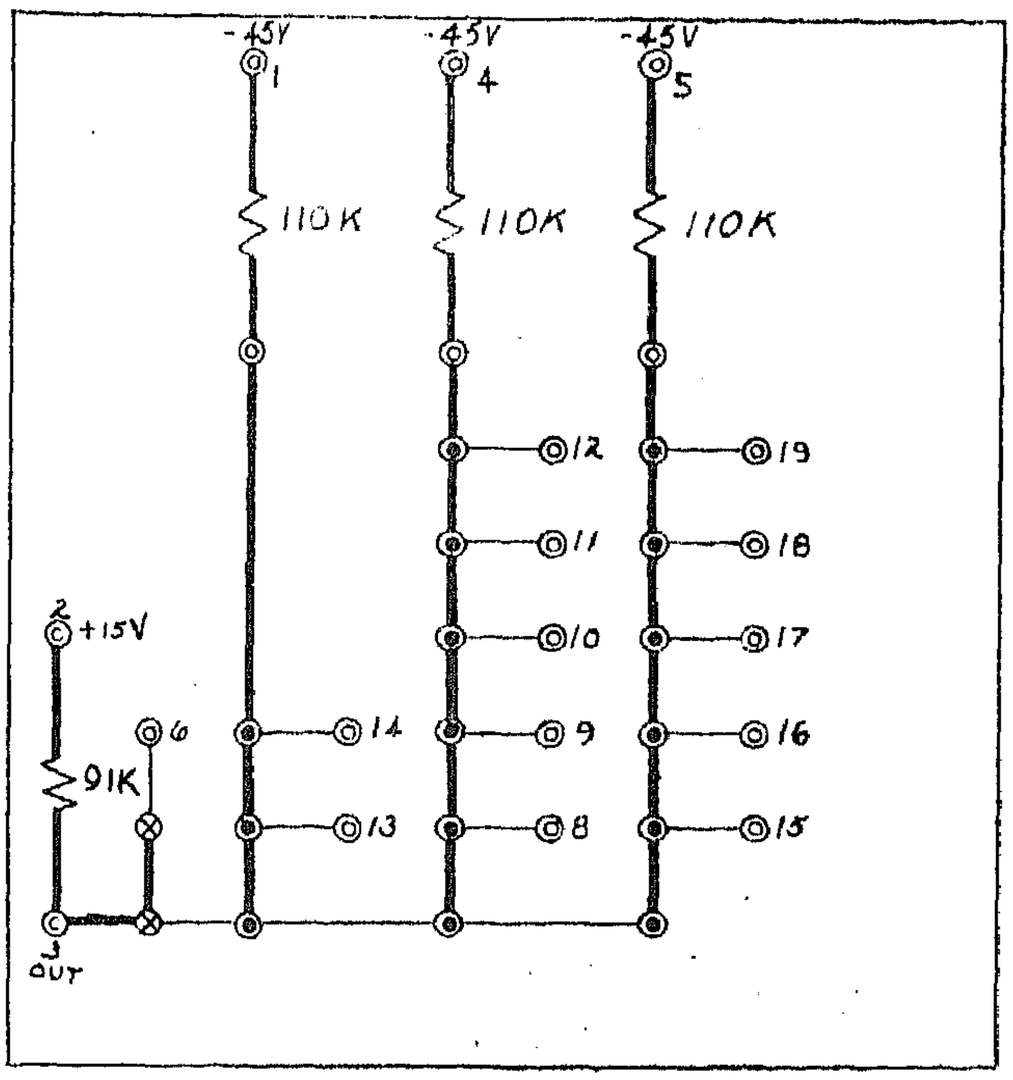
MARK IV	CC — C 13		SHEET NO.
	CODE	NUMBER	NO. OF SHEETS

Fig. 4-85



LEGEND:

- ◉ BRIGHT SIDE OF RECTIFIER
- ⊗ DULL SIDE OF RECTIFIER
- —— BACK CONNECTION
- ▬▬ FRONT CONNECTION

NOTE:

USE 0.4 TO 0.6 MA. FORWARD CURRENT RECTIFIERS.

(2,5,5)

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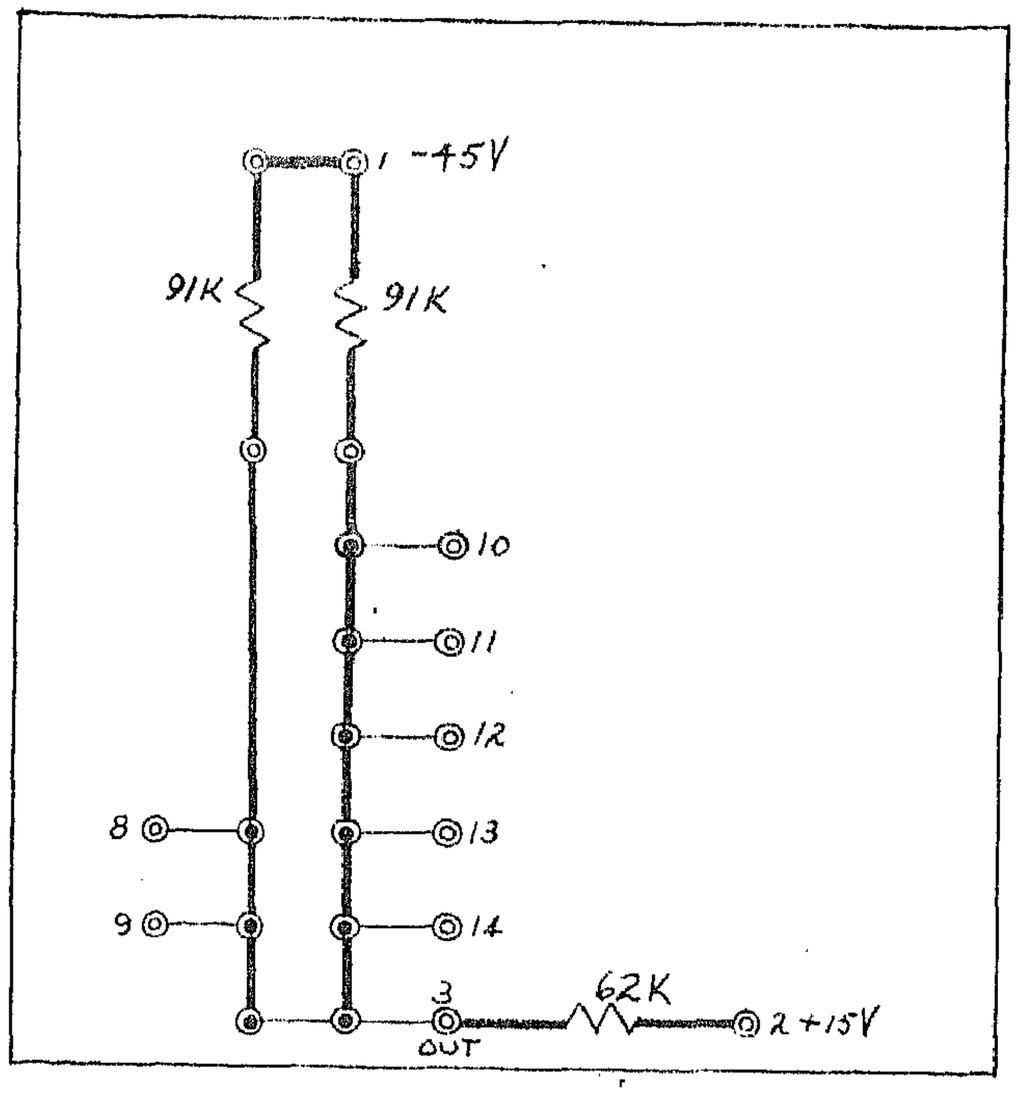
MARK IV	CC (CODE) — E17d (NUMBER)		SHEET NO.
			NO. OF SHEETS

Fig. 4-86



LEGEND:

⊙ BRIGHT SIDE OF RECTIFIER
⊗ DULL SIDE OF RECTIFIER
—— BACK CONNECTION
▬▬ FRONT CONNECTION

NOTE:

USE 0.4 TO 0.6 MA.
FORWARD CURRENT
RECTIFIERS.

(2, 5)

DATE: 6/30/51	DR. G L P	CH.	APP.
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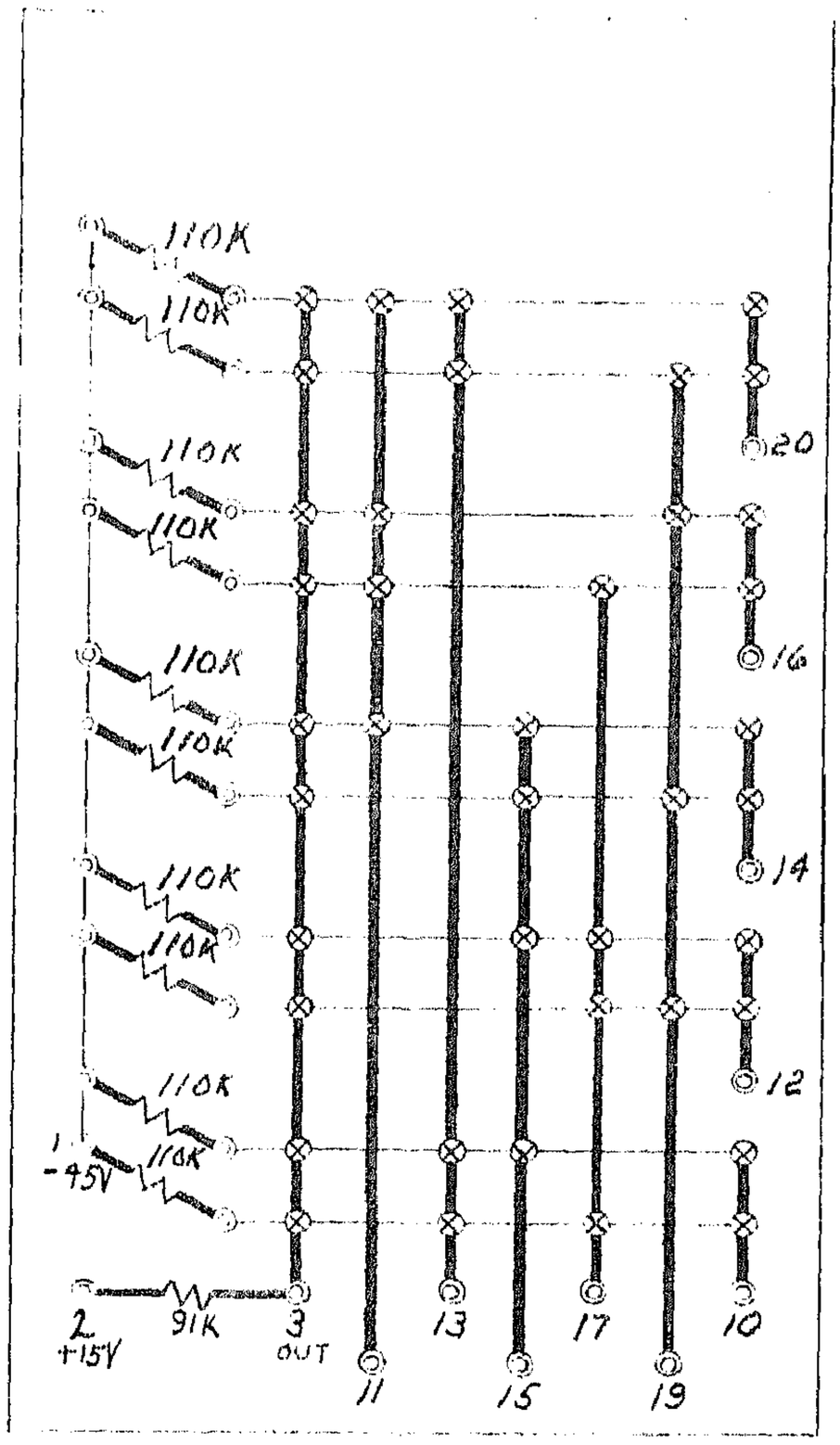
MARK IV	CC (CODE) — E-20 (NUMBER)	SHEET NO. 1	NO. OF SHEETS 1

Fig. 4-87



Legend:

⊗ Dull Side Of Rectifier

◎ Terminal Eyelet

Back Connection

Front Connection

Note:

Use 0.4 To 0.6 ma. Forward Current Rectifiers

REV.	DATE	BY	CHANGE

DATE 3-2-51 | DR. RJR | CH. | APP.

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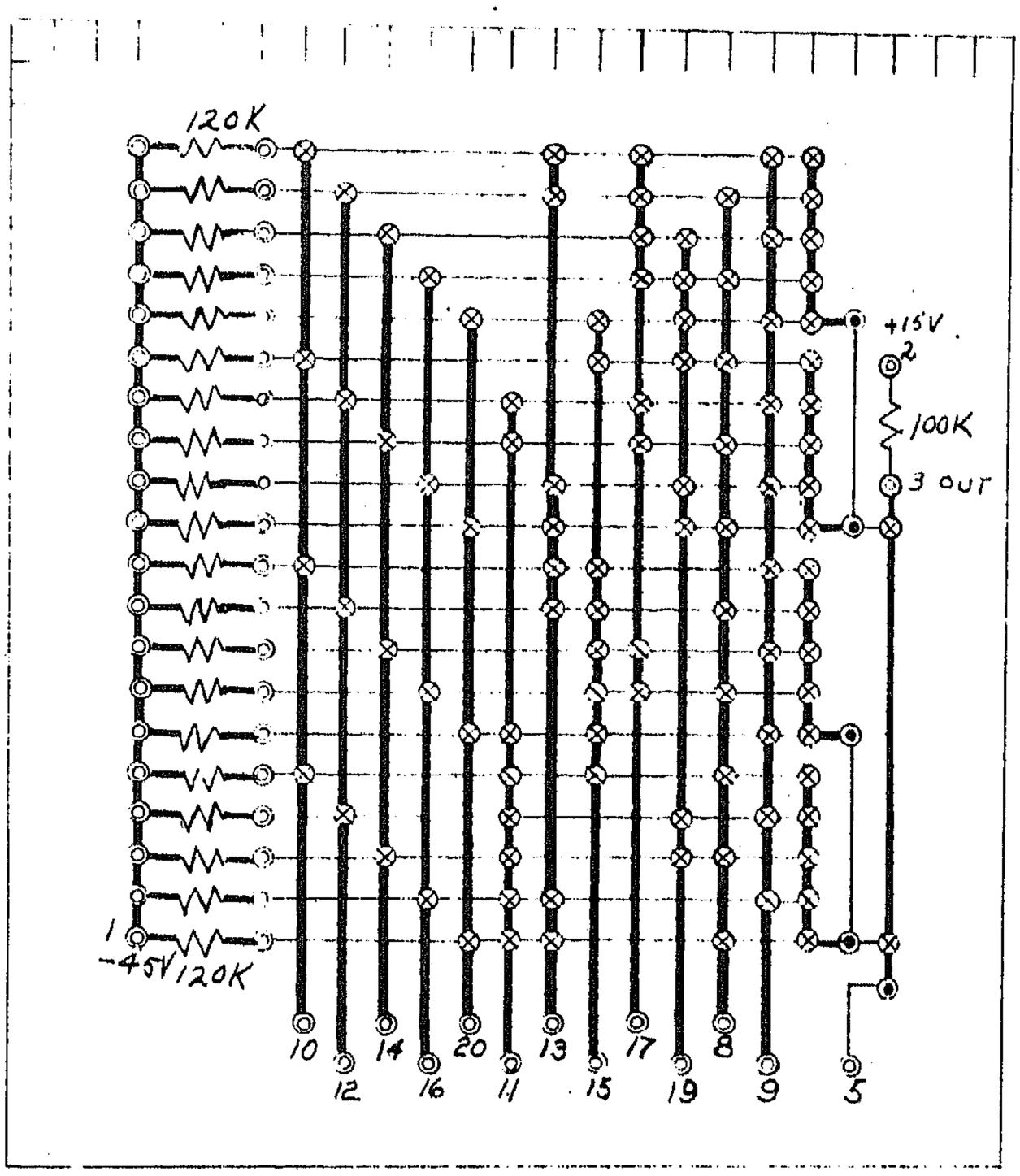
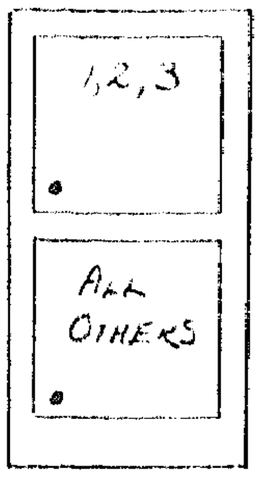
MARK IV | CC — S-3 (CODE — NUMBER) | SHEET NO. 1 | NO. OF SHEETS 1

Fig. 4-88



Bottom View
of
3115.T



Legend:
- ⊙ Bright Side Of Rectifier
- ⊗ Dull Side Of Rectifier
- ◎ Terminal Eyelet
- ——— Front Connection
- - - Back Connection

Note-1:
110 K Resistors Are To Be Connected Between Corresponding Terminal Eyelets Of Columns C & f.

Note-2:
Use 0.4 To 0.6 Forward Current Rectifiers

REV.	DATE	BY	CHANGE

DATE: 2·28·51 | DR. RJR | CH. | APP.

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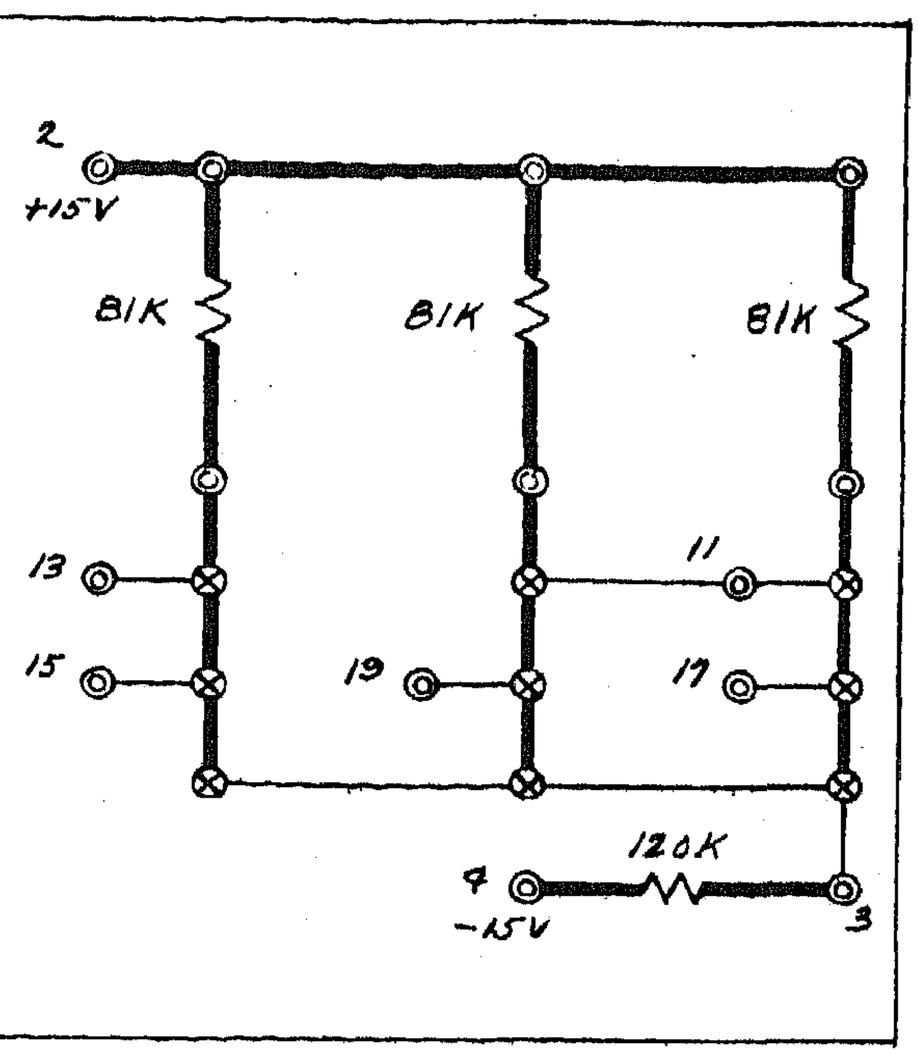
MARK IV | CC (CODE) — S-6 (NUMBER) | SHEET NO. 1 | NO. OF SHEETS 1

Fig. 4-89



REV.	DATE	BY	CHANGE

DATE: 6-6-51 | DR. R. D. | CH. | APP.

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MARK IV | C.C. CODE | — 5-12 NUMBER | SHEET NO. | NO. OF SHEETS

Fig. 4-90

APPENDIX 1

SYMBOLS USED IN CHAPTERS 3 AND 4

		Page
AO	Add One	4-13
βCAR	β Code Advance Reset	4-35
CA	Code Advance	4-34
CC	Condition Register	4-32
CRA	Call Register Advance	4-33
DRUMLU	Drum, Lower Unit's (0-4)	4-15
DS,DS'	Delay Line S, S' Advance Control	3-21
DSL,U	Delay Line S Upper 5, Lower 5	3-21
DT	Digit Time	3-1
E	Even	4-5
FIB	Fast In-Bus	3-1
FOB	Fast Out-Bus	3-1
FSR	First Sequence Trigger Pair Reset	4-25
FSRI	First Sequence Trigger Pair Read-In	4-27
FSTP	First Sequence Trigger Pair	4-24
γCAR	γ Code Advance Reset	4-35
γTRA	γ Transfer Register Advance	4-37
γTRL1	γ Transfer Register, Special Core Advance 1	4-37
γTRL2	γ Transfer Register, Special Core Advance 2	4-37
HR	Hundred's Relay	3-11
ICTR	I Control Register	4-25
IJKO	I,J,K Register Out	4-32
IJKR	I,J,K Control Reset	4-28
IJKRO	I,J,K Register Read-Out	4-32
JCTR	J Control Register	4-25
JRI	J Register Read-In	4-31
KCTR	K Control Register	4-25
LCTR	L Counter	4-25
LNCO	Line Number, Code Out	4-57
LNR	Line Number Register	4-5
LNRHE	Line Number Register, Hundred's Even	4-12
LNRHO	Line Number Register, Hundred's Odd	4-12
LNRLU	Line Number Register, Lower Unit's (0-4)	4-21
LNRMU	Line Number Register, Middle Unit's (3-7)	4-21
LNRRI	Line Number Register, Read-In	4-13
LNRT	Line Number Register, Ten's	4-11
LNRTHE	Line Number Register, Thousand's Even	4-12

		Page
LNRTHO	Line Number Register, Thousand's Odd	4-12
LNRU	Line Number Register, Unit's	4-11
m	Match Number Time	3-16
M	Match Phase and Number Time	3-16
MCO	Manual Controls Out	4-61
MCR	Main Control Ring	4-41
MCTR	M Counter	4-25
NRO	Number Read-Out	4-56
NT	Number Time	3-1
OD	S,S' Out to Drum	3-21
ODP	Operating Decimal Point	4-7
OS	S,S' Out to Storage	3-21
P	Phase	3-16
PP	Pole Piece Selection Trigger Pair	4-14
PUB7	Pick Up B7	4-50
PUN2	Pick Up N2	4-50
Q	Quadrant	4-5
R	Reset LNR Unit's and Ten's	4-13
RDB	Tape Read Busy	4-52
REC	Record Sequence Code	4-30
REH	Reset LNR Even Hundred's	4-13
RETH	Reset LNR Even Thousand's	4-13
RIS	Read-In Switch	4-62
RO	Reset LNR Odd Hundred's and Thousand's	4-13
RRI	Record Ring Advance	4-77
RS,RS'	Register S,S' Read-In	3-21
RST	Read Sequence Tape	4-52
S	Stop Register	4-46
SAL	Start Line Number	4-7
SCRH	Slow Storage Control Register Hundred's	3-8
SCRO	Slow Storage Control Register, Read-Out	3-10
SCRR	Slow Storage Control Register, Reset	3-8
SCRRI	Slow Storage Control Register, Read-In	3-8
SCRT	Slow Storage Control Register, Ten's	3-8
SCRTH	Slow Storage Control Register, Thousand's	3-8
SCRU	Slow Storage Control Register, Unit's	3-8
SM	Stop Match	4-47
SOL	Stop Line Number	4-7
SR	Slow Storage Ring	3-14
SRH	Slow Storage Ring Home	3-17
SSRR	Slow Storage Read-Record Register	3-17
SSTP	Second Sequence Trigger Pair	4-34
SSTPR	Second Sequence Trigger Pair Reset	4-34
SS200	Slow Storage Registers 200-209	3-17
SS210	Slow Storage Registers 210-219	3-17
ST	Slow Storage Triplet	3-17

		Page
THR	Thousand's Relay	3-11
XT	External Transfer	4-38
XTC	External Transfer Code	4-37
XTO	External Transfer Out	4-37
XTRA	External Transfer Register Advance	4-38